# XCM520 Series

ETR2427-004a

## 600mA Synchronous Step-Down DC/DC Converter + Dual LDO Regulator

## ■GENERAL DESCRIPTION

The XCM520 series is a multi chip module which comprises of a 600mA driver transistor built-in synchronous step–down DC/DC converter and a dual CMOS LDO regulator. The device is housed in small USP-12B01 package which is ideally suited for space conscious applications.

The XCM520 can replace this dual DC/DC to eliminate one inductor and reduce output noise.

The DC/DC converter with a built-in 0.42Ω P-channel MOS and a 0.52Ω N-channel MOS provides a high efficiency, stable power supply up to 600mA to using only a coil and two ceramic capacitors connected externally.

The highly accurate, low noise, dual CMOS LDO regulator includes a reference voltage source, error amplifiers, driver transistors, current limiters and phase compensation circuits internally. The series is also fully compatible with low ESR ceramic capacitors.

This high level of output stability is maintained even during frequent load fluctuations, due to the excellent transient response performance and high PSRR achieved across a broad range of frequencies. The EN function allows the output of each regulator to be turned off independently, resulting in greatly reduced power consumption.

## ■APPLICATIONS

●Close-proximity wireless transfer Module

## ■FEATURES

**<DC/DC Convertor Block>**

**Driver Transistor** : 0.42Ω P-channel MOS Built-in
**Switching Transistor** : 0.52Ω N-channel MOS Built-in
**Input Voltage Range** : 2.7V ～ 6.0V
**Output Voltage** : 2.3V($V_{OUT3}$)
**High Efficiency** : 86% (TYP.) *
**Output Current** : 600mA
**Oscillation Frequency** : 3.0MHz (±15%)
**Soft-Start** : Built-In Soft-Start
**Current Limiter Circuit** : Constant Current & Latching
**Control** : Fixed PWM, Auto PWM/PFM

*Performance depends on external components and wiring on PCB wiring.

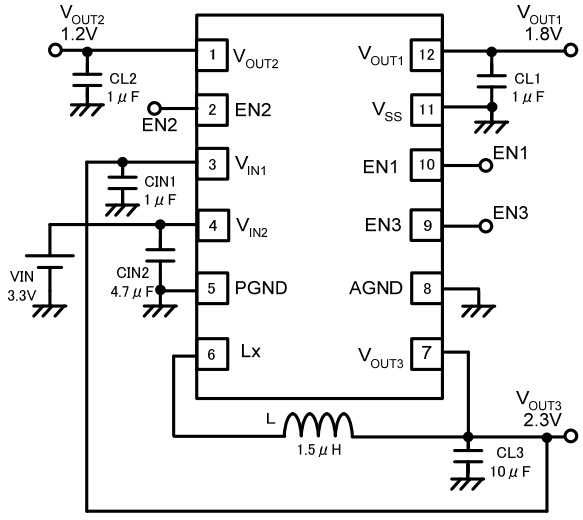
**<Dual LDO Regulator Block>**

**Maximum Output Current** : 150mA (Limiter 300mA TYP.)
**Dropout Voltage** : 100mV @ 100mA
**Operating Voltage Range** : 1.5V~6.0V
**Output Voltages** : 1.8V($V_{OUT1}$),1.2V($V_{OUT2}$)
**High Accuracy** : ±2%($V_{OUT1}$), ±30mV ($V_{OUT2}$)
**Low Power Consumption** : 25μA (TYP.)
**Stand-by Current** : Less than 0.1μA(TYP.)
**High Ripple Rejection** : 70dB @1kHz
**Low Output Noise**
**Operating Temperature Range** : -40℃~+85℃
**Low ESR Capacitor** : Ceramic Capacitor Compatible
**Package** : USP-12B01

| **Standard Voltage Combinations** | : $V_{OUT1}$ | $V_{OUT2}$ | $V_{OUT3}$ |
|---|---|---|---|
| XCM520AA01DR-G | | 1.8V | 1.2V | 2.3V |

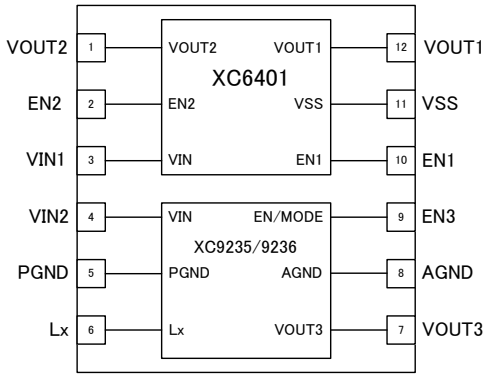
**Environmentally Friendly** : EU RoHS Compliant, Pb Free

## ■TYPICAL APPLICATION CIRCUIT



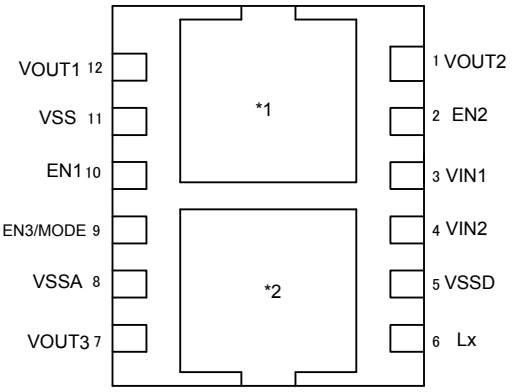

* The above circuit uses XCM520AA01DR-G.
* The DC/DC block $V_{OUT3}$ is connected to the dual LDO regulator $V_{IN1}$ in this connection.

## ■PIN CONFIGURATIOIN




(TOP VIEW)

| PIN No | XCM520 | XC6401 | XC9235/XC9236 |
|---|---|---|---|
| 1 | $V_{OUT2}$ | $V_{OUT2}$ | — |
| 2 | EN2 | EN2 | — |
| 3 | $V_{IN1}$ | $V_{IN}$ | — |
| 4 | $V_{IN2}$ | — | $V_{IN}$ |
| 5 | PGND | — | PGND |
| 6 | Lx | — | Lx |
| 7 | $V_{OUT3}$ | — | $V_{OUT}$ |
| 8 | AGND | — | AGND |
| 9 | EN3 | — | CE |
| 10 | EN1 | EN1 | — |
| 11 | $V_{SS}$ | $V_{SS}$ | — |
| 12 | $V_{OUT1}$ | $V_{OUT1}$ | — |




(TOP VIEW)

NOTE:
* The two heat-sink pads on the back side are electrically isolated in the package.
*1: The pad of the regulator should be $V_{SS}$ level.
*2: The pad of the DC/DC should be $V_{SS}$ level.
* The DC/DC ground pin (No. 5 and 8) should be connected for use.
* The two pads are recommended to open on the board, but care must be taken for voltage level of each heat-sink pad when they are electrically connected.

## ■PIN ASSIGNMENT

| PIN No | XCM520 | FUNCTIONS |
|---|---|---|
| 1 | $V_{OUT2}$ | Voltage Regulator Output2 |
| 2 | EN2 | Voltage Regulator ON/OFF Control 2 |
| 3 | $V_{IN1}$ | Voltage Regulator Power Input |
| 4 | $V_{IN2}$ | DC/DC Power Input |
| 5 | PGND | DC/DC Power Ground |
| 6 | Lx | DC/DC Inductor Pin |
| 7 | $V_{OUT3}$ | DC/DC Output Voltage |
| 8 | AGND | DC/DC Analog Ground |
| 9 | EN3 | DC/DC ON/OFF Control |
| 10 | EN1 | Voltage Regulator ON/OFF Control 1 |
| 11 | $V_{SS}$ | Voltage Regulator Ground |
| 12 | $V_{OUT1}$ | Voltage Regulator Output Voltage 1 |

# ■PRODUCT CLASSIFICATION

●Ordering Information

XCM520①②③④⑤⑥-⑦(*1)

| DESIGNATOR | DESCRIPTION | SYMBOL | DESCRIPTION |
|---|---|---|---|
| ①② | Options | － | See the chart below |
| ③④ | Output Voltage combination | － | See the chart below |
| ⑤⑥-⑦ | Packages<br>Taping Type (*2) | DR-G | USP-12B01 |

(*1) The “-G” suffix indicates that the products are Halogen and Antimony free as well as being fully RoHS compliant.

(*2) The device orientation is fixed in its embossed tape pocket. For reverse orientation, please contact your local Torex sales office or representative. (Standard orientation: ⑤R-⑦, Reverse orientation: ⑤L-⑦)

●DESIGNATOR①②（Combination of XC6401 series and XC9235/XC9236 series）

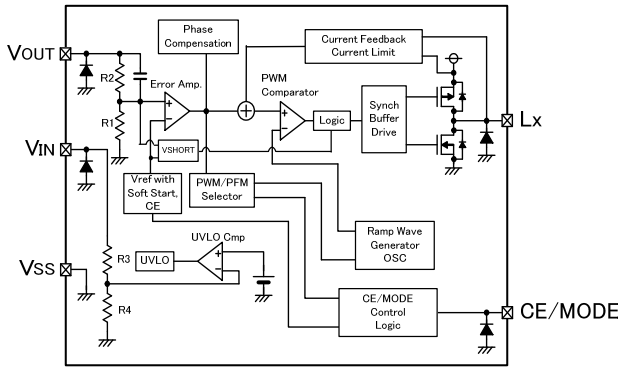
| ①② | COMBINATION OF EACH IC | DESCRIPTION |
|---|---|---|
| AA | XC6401FF**＋XC9235A**D | Fixed PWM, $f_{OSC}$=3.0MHz |

●DESIGNATOR③④（Output Voltage）

| ③④ | $V_{OUT1}$(VR_1ch) | $V_{OUT2}$(VR_2ch) | $V_{OUT3}$(DC/DC) |
|---|---|---|---|
| 01 | 1.8 | 1.2 | 2.3 |

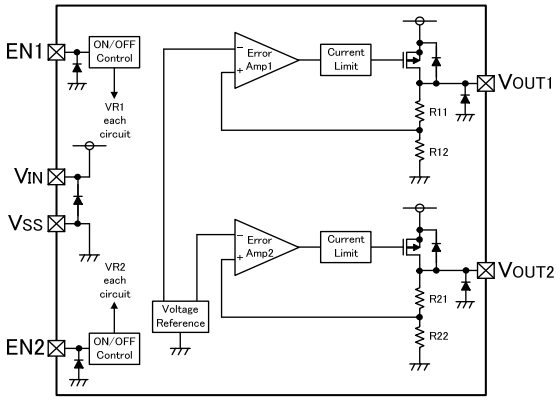
## ■BLOCK DIAGRAMS

XC9235A




* XC9235 control scheme is a fixed PWM because that the “CE/MODE Control Logic” outputs a low level signal to the “PWM/PFM Selector”.

XC6401FF




*Diodes inside the circuit are an ESD protection diode and a parasitic diode.

## ■MAXIMUM ABSOLUTE RATINGS

| PARAMETER | | SYMBOL | RATINGS | UNITS |
|---|---|---|---|---|
| $V_{IN1}$ Voltage | | $V_{IN1}$ | 6.5 | V |
| $V_{OUT}$ Current | | $I_{OUT1}+I_{OUT2}$ *1 | 700 *2 | mA |
| $V_{OUT}$ Voltage | | $V_{OUT1}$ / $V_{OUT2}$ | $V_{SS}$-0.3～$V_{IN1}$+0.3 | V |
| EN1,EN2 Voltage | | $V_{EN1}$ / $V_{EN2}$ | $V_{SS}$-0.3～6.5 | V |
| $V_{IN2}$ Voltage | | $V_{IN2}$ | -0.3～6.5 | V |
| Lx Voltage | | $V_{LX}$ | -0.3～$V_{IN2}$+0.3≦6.5 | V |
| $V_{OUT3}$ Voltage | | $V_{OUT3}$ | -0.3～6.5 | V |
| EN3 Voltage | | $V_{EN3}$ | -0.3～6.5 | V |
| Lx Current | | $I_{LX}$ | ±1500 | mA |
| Power Dissipation | USP12-B01 | Pd | 150 | mW |
| | USP12-B01 *3 (PCB mounted) | | 800 (1ch operate) | |
| | | | 600 (both 2ch operate) | |
| Operating Temperature Range | | Topr | -40～+85 | ℃ |
| Storage Temperature Range | | Tstg | -55～+125 | ℃ |

*1. Rating is defined as a total of VR1 and VR2 in the VR bloc.

*2. Pd > { ($V_{IN1}$ - $V_{OUT1}$)×$I_{OUT1}$+($V_{IN1}$ - $V_{OUT2}$)×$I_{OUT2}$ }

*3. The power dissipation figure shown is PCB mounted. Please refer to page 41 for details. Also, the power dissipation value above is for each channel.

# ■ELECTRICAL CHARACTERISTICS (Continued)

●XCM520AA/AC (DC/DC BLOCK) $V_{OUT3}$ = 2.3V, $f_{OSC}$= 3.0MHz, Ta=25℃

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{OUT3}$ | When connected to external components, $V_{IN2}$ = $V_{EN3}$ = 5.0V, $I_{OUT3}$ = 30mA | 2.254 | 2.300 | 2.346 | V | ① |
| Operating Voltage Range | $V_{IN2}$ | | 2.7 | - | 6.0 | V | ① |
| Maximum Output Current | $I_{OUT3MAX}$ | When connected to external components, $V_{IN2}$=$V_{OUT3(E)}$+2.0V, $V_{EN3}$=1.0V (*8) | 600 | - | - | mA | ① |
| UVLO Voltage | $V_{UVLO}$ | $V_{EN3}$ = $V_{IN2}$ , $V_{OUT3}$ = 0V , Voltage which Lx pin holding "L" level (*1, *10) | 1.00 | 1.40 | 1.78 | V | ② |
| Supply Current | $I_{DD}$ | $V_{IN2}$=$V_{EN3}$=5.0V,$V_{OUT3}$=$V_{OUT3(E)}$ × 1.1V | - | 46 | 65 | μA | ③ |
| Stand-by Current | $I_{STB}$ | $V_{IN2}$ = 5.0V, $V_{EN}$ = 0V, $V_{OUT3}$ = $V_{OUT3(E)}$ × 1.1V | - | 0 | 1.0 | μA | ③ |
| Oscillation Frequency | $f_{OSC}$ | When connected to external components, $V_{IN2}$ = $V_{OUT3(E)}$ + 2.0V , $V_{EN3}$=1.0V, $V_{OUT3}$ = 100mA | 2550 | 3000 | 3450 | kHz | ① |
| PFM Switching Current | $I_{PFM}$ | When connected to external components, $V_{IN2}$ = $V_{OUT3(E)}$ + 2.0V, $V_{EN3}$ = $V_{IN2}$ , $I_{OUT3}$ = 1mA (*11) | 170 | 220 | 270 | mA | ① |
| PFM Duty Limit | $DTY_{LIMIT\_PFM}$ | $V_{EN3}$ = $V_{IN2}$ = (C-1) $I_{OUT3}$ = 1mA (*11) | | 200 | 300 | % | ② |
| Maximum Duty Ratio | $D_{MAX}$ | $V_{IN2}$ = $V_{EN3}$ = 5.0V, $V_{OUT3}$ = $V_{OUT3\,(E)}$ × 0.9V | 100 | - | - | % | ② |
| Minimum Duty Ratio | $D_{MIN}$ | $V_{IN2}$ = $V_{EN3}$ = 5.0V, $V_{OUT3}$ = $V_{OUT3\,(E)}$ × 1.1V | - | - | 0 | % | ② |
| Efficiency (*2) | EFFI | When connected to external components, $V_{EN3}$ = $V_{IN2}$ = $V_{OUT3\,(E)}$ + 1.2V, $V_{OUT3}$ = 100mA (*7) | - | 86 | - | % | ① |
| Lx SW "H" ON Resistance 1 | $R_{Lx\,H}$ | $V_{IN2}$ = $V_{EN3}$ = 5.0V, $V_{OUT3}$ = 0V, $IL_X$ = 100mA (*3) | - | 0.35 | 0.55 | Ω | ④ |
| Lx SW "H" ON Resistance 2 | $R_{Lx\,H}$ | $V_{IN2}$ = $V_{EN3}$ = 3.6V, $V_{OUT3}$ = 0V, $IL_X$ = 100mA (*3) | - | 0.42 | 0.67 | Ω | ④ |
| Lx SW "L" ON Resistance 1 | $R_{Lx\,L}$ | $V_{IN2}$ = $V_{EN3}$ =5.0V (*4) | - | 0.45 | 0.66 | Ω | — |
| Lx SW "L" ON Resistance 2 | $R_{Lx\,L}$ | $V_{IN2}$ = $V_{EN3}$ = 3.6V (*4) | - | 0.52 | 0.77 | Ω | — |
| Lx SW "H" Leak Current (*5) | $I_{LEAKH}$ | $V_{IN2}$ = $V_{OUT3}$ = 5.0V, $V_{EN3}$ = 0V, $L_X$= 0V | - | 0.01 | 1.0 | μA | ⑤ |
| Lx SW "L" Leak Current (*5) | $I_{LEAKL}$ | $V_{IN2}$ = $V_{OUT3}$ = 5.0V, $V_{EN3}$ = 0V, $L_X$= 5.0V | - | 0.01 | 1.0 | μA | ⑤ |
| Current Limit (*9) | $I_{LIM}$ | $V_{IN2}$ = $V_{EN3}$ = 5.0V, $V_{OUT3}$ = $V_{OUT3\,(E)}$ × 0.9V | 900 | 1050 | 1350 | mA | ⑥ |
| Output Voltage Temperature Characteristics | $\Delta V_{OUT3}$/ ($V_{OUT3}$ · $\Delta$topr) | $V_{OUT3}$ = 30mA -40℃ ≦ Topr ≦ 85℃ | - | ±100 | - | ppm/ ℃ | ① |
| EN "H" Level Voltage | $V_{ENH}$ | $V_{OUT3}$ =0V, Applied voltage to $V_{EN3}$, Voltage changes Lx to "H" level (*10) | 0.65 | - | 6.0 | V | ③ |
| EN "L" Level Voltage | $V_{EN3L}$ | $V_{OUT3}$ =0V, Applied voltage to $V_{EN3}$, Voltage changes Lx to "L" level (*10) | $V_{SS}$ | - | 0.25 | V | ③ |
| EN "H" Current | $I_{EN3H}$ | $V_{IN2}$ = $V_{EN3}$ =5.0V, $V_{OUT3}$ = 0V | - 0.1 | | 0.1 | μA | ⑤ |
| EN "L" Current | $I_{EN3L}$ | $V_{IN2}$ =5.0V, $V_{EN3}$ = 0V, $V_{OUT3}$ = 0V | - 0.1 | - | 0.1 | μA | ⑤ |
| Soft Start Time | $t_{SS}$ | When connected to external components, $V_{EN3}$ = 0V → $V_{IN2}$ , $V_{OUT3}$ = 1mA | 0.5 | 0.9 | 2.5 | ms | ① |
| Integral Latch Time | $t_{LAT}$ | $V_{IN2}$ = $V_{EN3}$ = 5.0V, $V_{OUT3}$ = 0.8 × $V_{OUT3\,(E)}$ Short Lx at 1Ω resistance (*6) | 1.0 | - | 20.0 | ms | ⑦ |
| Short Protection Threshold Voltage | $V_{SHORT}$ | Sweeping $V_{OUT3}$, $V_{IN2}$ = $V_{EN3}$ = 5.0V, Short Lx at 1Ω resistance, $V_{OUT3}$ voltage which Lx becomes "L" level within 1ms | 0.675 | 0.900 | 1.125 | V | ⑦ |

Test conditions: Unless otherwise stated, $V_{IN2}$ = 5.0V, $V_{OUT3\,(E)}$ = Nominal voltage

NOTE:

*1: Including hysteresis width of operating voltage.

*2: EFFI = { ( output voltage × output current ) ／ ( input voltage × input current) } × 100

*3: ON resistance (Ω)= ($V_{IN}$ - Lx pin measurement voltage) ／ 100mA

*4: Design value

*5: When temperature is high, a current of approximately 10μA (maximum) may leak.

*6: Time until it short-circuits $V_{OUT3}$ with GND via 1Ω of resistor from an operational state and is set to Lx=0V from current limit pulse generating.

*7: $V_{OUT3\,(E)}$+1.2V<2.7V, $V_{IN2}$=2.7V.

*8: When the difference between the input and the output is small, some cycles may be skipped completely before current maximizes. If current is further pulled from this state, output voltage will decrease because of P-ch driver ON resistance.

*9: Current limit denotes the level of detection at peak of coil current.

*10: "H"＝$V_{IN2}$～$V_{IN2}$ - 1.2V, "L"＝+ 0.1V ～ - 0.1V

*The electrical characteristics above are when the voltage regulator block is in stop.

## ■ELECTRICAL CHARACTERISTICS (Continued)

●XCM520 Series VR Block (VR1/VR2: EN_ Active High, without Pull-down resistors) Ta=25℃

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{OUT(E)}$ (*2) | $I_{OUT}$=30mA | $V_{OUT(T)}$≧1.5V | X0.98 (*3) | $V_{OUT(T)}$ (*4) | X1.02 (*3) | V | ⑩ |
| | | | $V_{OUT(T)}$<1.5V | -0.03 (*3) | | +0.03 (*3) | | |
| Maximum Output Current | $I_{OUTMAX}$ | $V_{IN1}$=$V_{OUT(T)}$ + 1.0V | | 150 | - | - | mA | ⑩ |
| Load Regulation | $\Delta V_{OUT}$ | 1mA≦$I_{OUT}$≦100mA | | - | 15 | 60 | mV | ⑩ |
| Dropout Voltage (*5) | Vdif1 | $I_{OUT}$=30mA | | E-1 | | | mV | ⑩ |
| | Vdif2 | $I_{OUT}$=100mA | | E-2 | | | mV | |
| Supply Current | $I_{SS}$ | $V_{IN1}$=$V_{EN}$=$V_{OUT(T)}$ + 1.0V, $I_{OUT}$=0mA | | - | 25 | 45 | μA | ⑫ |
| Stand-by Current | $I_{STB}$ | $V_{IN1}$=$V_{OUT(T)}$ + 1.0V, $V_{EN}$=$V_{SS}$ | | - | 0.01 | 0.10 | μA | ⑪ |
| Input Regulation (*8) | $\Delta V_{OUT}$ / | $V_{OUT(T)}$+1.0V≦$V_{IN1}$≦6.0V | | - | 0.01 | 0.20 | % / V | ⑩ |
| | ($\Delta V_{IN1}$ ・ $V_{OUT}$) | $V_{EN}$=$V_{IN1}$, $I_{OUT}$=30mA | | | | | | |
| Input Voltage | $V_{IN1}$ | | | 1.5 | - | 6.0 | V | - |
| Output Voltage Temperature Characteristics | $\Delta V_{OUT}$ / | $I_{OUT}$=30mA | | - | ±100 | - | ppm/℃ | ⑩ |
| | ($\Delta$Topr ・$V_{OUT}$) | -40℃≦Topr≦85℃ | | | | | | |
| Ripple Rejection (*9) | PSRR | $V_{IN1}$=[$V_{OUT(T)}$+1.0]VDC+0.5Vp-pAC<br>$I_{OUT}$=30mA, f=1kHz | | - | 70 | - | dB | ⑬ |
| Limit Current | $I_{LIM}$ | $V_{IN1}$=$V_{OUT(T)}$ + 1.0V, $V_{EN}$=$V_{IN1}$ | | - | 300 | - | mA | ⑩ |
| Short Current | $I_{SHORT}$ | $V_{IN1}$=$V_{OUT(T)}$ + 1.0V, $V_{EN}$=$V_{IN1}$ | | - | 30 | - | mA | ⑩ |
| EN "H" Level Voltage | $V_{ENH}$ | | | 1.30 | - | 6 | V | ⑭ |
| EN "L" Level Voltage | $V_{ENL}$ | | | - | - | 0.25 | V | ⑭ |
| EN "H" Level Current | $I_{ENH}$ | $V_{IN1}$=$V_{EN}$=$V_{OUT(T)}$ + 1.0V | | -0.10 | - | 0.10 | μA | ⑭ |
| EN "L" Level Current | $I_{ENL}$ | $V_{IN1}$= $V_{OUT(T)}$ + 1.0V, $V_{EN}$=$V_{SS}$ | | -0.10 | - | 0.10 | μA | ⑭ |

NOTE:

*1 : Unless otherwise stated, $V_{IN1}$=$V_{OUT(T)}$+1.0V

*2 : $V_{OUT(E)}$ : Effective output voltage

(I.e. the output voltage when "$V_{OUT(T)}$＋1.0V" is provided at the $V_{IN}$ pin while maintaining a certain $I_{OUT}$ value).

*3 : Please see the Voltage Chart for each voltage of $V_{OUT(E)}$. If $V_{OUT(T)}$≦1.45V, MIN $V_{OUT(T)}$ - 30mV, MAX $V_{OUT(T)}$ + 30mV

*4 : $V_{OUT(T)}$ : Nominal output voltage

*5 : Vdif={$V_{INa}$(*7)-$V_{OUTa}$(*6)}

*6 : $V_{OUT1}$=A voltage equal to 98% of the output voltage whenever an amply stabilized $I_{OUT}$ {$V_{OUT(T)}$+1.0V} is input.

*7 : $V_{IN1}$=The input voltage when $V_{OUT1}$ appears as input voltage is gradually decreased.

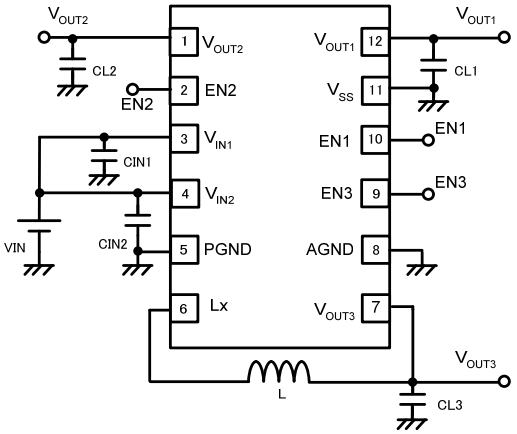
*The electrical characteristics above are when the DC/DC block is in stop.

## ■OUTPUT VOLTAGE CHART

●Voltage Chart 1

| NOMINAL OUTPUT VOLTAGE | OUTPUT VOLTAGE (V) | | E-1 | | E-2 | |
|---|---|---|---|---|---|---|
| | | | DROPOUT VOLTAGE 1 (mV) | | DROPOUT VOLTAGE 2 (mV) | |
| $V_{OUT(T)}$ | $V_{OUT}$ | | Vdif1 | | Vdif2 | |
| | MIN. | MAX. | TYP. | MAX. | TYP. | MAX. |
| 1.20 | 1.170 | 1.230 | 65 | 300 | 200 | 400 |
| 1.80 | 1.764 | 1.836 | 45 | 65 | 140 | 180 |

# ■TYPICAL APPLICATION CIRCUIT




● DC/DC BLOCK $f_{OSC}$=3.0MHz

| | | | |
|---|---|---|---|
| $C_{IN1}$ | : | 1μF | (Ceramic) |
| $C_{L1}$ | : | 1μF | (Ceramic) |
| $C_{L2}$ | : | 1μF | (Ceramic) |
| L | : | 1.5μH | (NR3015 TAIIYO YUDEN) |
| $C_{IN2}$ | : | 4.7μF | (Ceramic) |
| $C_{L3}$ | : | 10μF | (Ceramic) |

# ■OPERATIONAL EXPLANATION

●DC/DC BLOCK

The DC/DC block of the XCM520 series consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, output voltage adjustment resistors, P-channel MOSFET driver transistor, N-channel MOSFET switching transistor for the synchronous switch, current limiter circuit, UVLO circuit and others. (See the block diagram above.)

By using the error amplifier, the voltage of the internal voltage reference source is compared with the feedback voltage from the $V_{OUT3}$ pin through split resistors, R1 and R2. Phase compensation is performed on the resulting error amplifier output, to input a signal to the PWM comparator to determine the turn-on time during PWM operation. The PWM comparator compares, in terms of voltage level, the signal from the error amplifier with the ramp wave from the ramp wave circuit, and delivers the resulting output to the buffer driver circuit to cause the Lx pin to output a switching duty cycle. This process is continuously performed to ensure stable output voltage.

The current feedback circuit monitors the P-channel MOS driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor such as a ceramic capacitor is used ensuring stable output voltage.

<Reference Voltage Source>

The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Ramp Wave Circuit>

The ramp wave circuit determines switching frequency. The frequency is fixed internally and can be selected from 1.2MHz or 3.0MHz. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<Error Amplifier>

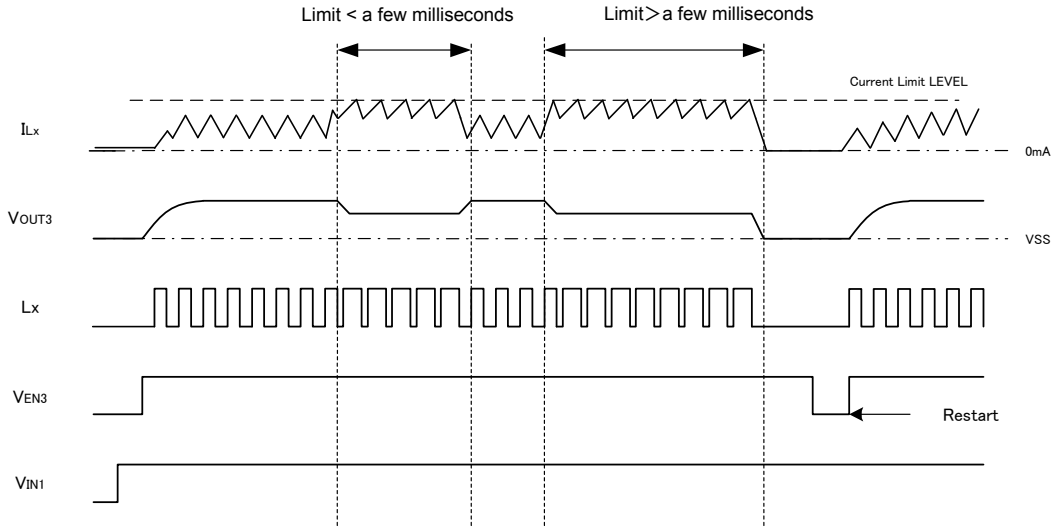
The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal split resistors, R1 and R2. When a voltage is lower than the reference voltage is fed back, the output voltage of the error amplifier increases. The gain and frequency characteristics of the error amplifier output are fixed internally to deliver an optimized signal to the mixer.

## ■OPERATIONAL EXPLANATION (Continued)

<Current Limit>
The current limiter circuit of the XCM520 series monitors the current flowing through the P-channel MOS driver transistor connected to the Lx pin, and features a combination of the current limit mode and the operation suspension mode.

① When the driver current is greater than a specific level, the current limit function operates to turn off the pulses from the Lx pin at any given timing.
② When the P-channel MOS driver transistor is turned off, the limiter circuit is then released from the current limit detection state.
③ At the next pulse, the P-channel MOS driver transistor is turned on. However, the P-channel MOS driver transistor is immediately turned off in the case of an over current state.
④ When the over current state is eliminated, the IC resumes its normal operation.

The IC waits for the over current state to end by repeating the steps ① through ③. If an over current state continues for a few milliseconds and the above three steps are repeatedly performed, the IC performs the function of latching the OFF state of the P-channel MOS driver transistor, and goes into operation suspension mode. Once the IC is in suspension mode, operations can be resumed by either turning the IC off via the EN3 pin, or by restoring power to the $V_{IN2}$ pin. The suspension mode does not mean a complete shutdown, but a state in which pulse output is suspended; therefore, the internal circuitry remains in operation. The current limit of the XCM520 series can be set at 1050mA at typical. Besides, care must be taken when laying out the PC Board, in order to prevent miss-operation of the current limit mode. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.



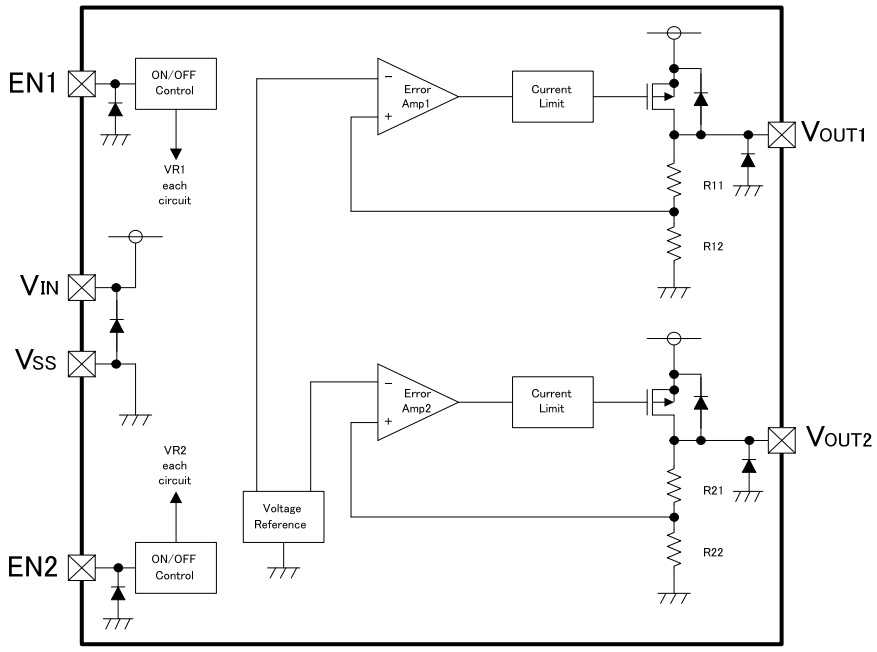

<Short-Circuit Protection>
The short-circuit protection circuit monitors the internal R1 and R2 divider voltage from the $V_{OUT3}$ pin. In case where output is accidentally shorted to the ground and when the FB point voltage decreases less than half of the reference voltage (Vref) and a current more than the $I_{LIM}$ flows to the driver transistor, the short-circuit protection quickly operates to turn off and to latch the driver transistor. In latch state, the operation can be resumed by either turning the IC off and on via the EN3 pin, or by restoring power supply to the $V_{IN2}$ pin.
When sharp load transient happens, a voltage drop at the $V_{OUT3}$ pin is propagated to FB point through $C_{FB}$, as a result, short circuit protection may operate in the voltage higher than 1/2 $V_{OUT3}$ voltage.

<UVLO Circuit>
When the $V_{IN2}$ pin voltage becomes 1.4V or lower, the P-channel MOS driver transistor is forced OFF to prevent false pulse output caused by unstable operation of the internal circuitry. When the $V_{IN2}$ pin voltage becomes 1.8V or higher, switching operation takes place. By releasing the UVLO function, the IC performs the soft start function to initiate output startup operation. The soft start function operates even when the $V_{IN}$ pin voltage falls momentarily below the UVLO operating voltage. The UVLO circuit does not cause a complete shutdown of the IC, but causes pulse output to be suspended; therefore, the internal circuitry remains in operation.

# ■OPERATIONAL EXPLANATION (Continued)

## ●Voltage Regulator BLOCK

The voltage divided by resistors R1 and R2 is compared with the internal reference voltage by the error amplifier. The P-channel MOSFETs, which are connected to the VOUT pin, are then driven by the subsequent output signal. The output voltages at the VOUT pin is controlled and stabilized by a system of negative feedback. The current limit circuit and short protect circuit operate in relation to the level of output current. Further, the IC's internal circuitry can be shutdown via the EN pin's signal.




< Low ESR Capacitors >

With the XCM520 series, a stable output voltage is achievable even if used with low ESR capacitors as a phase compensation circuit is built-in. In order to ensure the effectiveness of the phase compensation, we suggest that output capacitor ($C_L$) is connected as close as possible to the output pins (VOUT) and the VSS pin. Please use an output capacitor with a capacitance value of at least 1 $\mu$F. Also, please connect an input capacitor ($C_{IN1}$) of 1 $\mu$F between the VIN1 pin and the VSS pin in order to ensure a stable power input.

< Current Limiter, Short-Circuit Protection >

The XCM520 series includes a combination of a fixed current limiter circuit and a fold-back circuit which aid the operations of the current limiter and circuit protection. When the load current reaches the current limit level, the fixed current limiter circuit operates and output voltage drops. As a result of this drop in output voltage, the fold-back circuit start to operate, output voltage drops further and output current decreases. When the output pin is shorted, a current of about 30mA flows.

< EN Pins >

The IC's internal circuitry can be shutdown via the signal from the EN pin with the XCM520 series. In shutdown state, output at the VOUT pin will be pulled down to the VSS level via R1 and R2. The operational logic of the IC's EN pin is selectable (please refer to the selection guide). Note that as the standard type's regulator 1 and 2 are both ' High Active/No Pull Down', operations will become unstable with the EN pin open. Although the EN pin is equal to an inverter input with CMOS hysteresis, with either the pull-up or pull-down options, the EN pin input current will increase when the IC is in operation. We suggest that you use this IC with either a VIN1 voltage or a VSS voltage input at the EN pin. If this IC is used with the correct specifications for the EN pin, the operational logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry.

## ■NOTES ON USE

<DC/DC BLOCK>

1. The XCM520 series is designed for use with ceramic output capacitors. If, however, the potential difference is too large between the input voltage and the output voltage, a ceramic capacitor may fail to absorb the resulting high switching energy and oscillation could occur on the output. If the input-output potential difference is large, connect an electrolytic capacitor in parallel to compensate for insufficient capacitance.

2. Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

3. As a result of input-output voltage and load conditions, oscillation frequency goes to 1/2, 1/3, and continues, then a ripple may increase.

4. When input-output voltage differential is large and light load conditions, a small duty cycle comes out. After that, 0%duty cycle may continue in several periods.

5. When input-output voltage differential is small and heavy load conditions, a large duty cycle comes out and may continues100% duty cycle in several periods.

6. With the IC, the peak current of the coil is controlled by the current limit circuit. Since the peak current increases when dropout voltage or load current is high, current limit starts operation, and this can lead to instability. When peak current becomes high, please adjust the coil inductance value and fully check the circuit operation. In addition, please calculate the peak current according to the following formula:
   $Ipk = (V_{IN2}-V_{OUT3})\times OnDuty /(2\times L\times f_{OSC}) + I_{OUT}$
   L: Coil Inductance Value
   $f_{OSC}$: Oscillation Frequency

7. When the peak current which exceeds limit current flows within the specified time, the built-in P-channel MOS driver transistor turns off. During the time until it detects limit current and before the built-in P-channel MOS driver transistor can be turned off, the current for limit current flows; therefore, care must be taken when selecting the rating for the external components such as a coil.

8. Depending on the state of the PC Board, latch time may become longer and latch operation may not work. In order to avoid the effect of noise, the board should be laid out so that input capacitors are placed as close to the IC as possible.

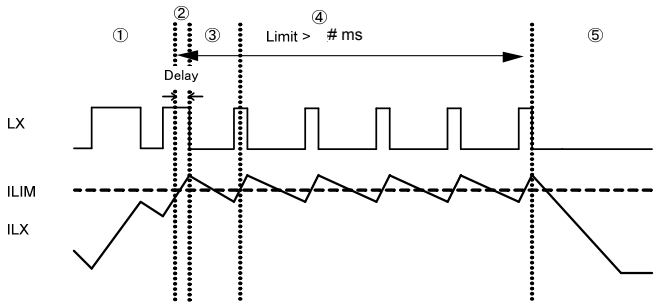
9. Use of the IC at voltages below the recommended voltage range may lead to instability.

10. This IC should be used within the stated absolute maximum ratings in order to prevent damage to the device.

11. When the IC is used in high temperature, output voltage may increase up to input voltage level at no load because of the leak current of the P-channel MOS driver transistor.

12. The current limit is set to 1350mA (MAX.) at typical. However, the current of 1350mA or more may flow.
    In case that the current limit functions while the $V_{OUT3}$ pin is shorted to the GND pin, when P-channel MOS driver transistor is ON, the potential difference for input voltage will occur at both ends of a coil. For this, the time rate of coil current becomes large. By contrast, when N-channel MOS driver transistor is ON, there is almost no potential difference at both ends of the coil since the $V_{OUT3}$ pin is shorted to the GND pin. Consequently, the time rate of coil current becomes quite small. According to the repetition of this operation, and the delay time of the circuit, coil current will be converged on a certain current value, exceeding the amount of current, which is supposed to be limited originally. Even in this case, however, after the over current state continues for several ms, the circuit will be latched. A coil should be used within the stated absolute maximum rating in order to prevent damage to the device.

    ①Current flows into P-channel MOS driver transistor to reach the current limit ($I_{LIM}$).
    ②The current of $I_{LIM}$ or more flows since the delay time of the circuit occurs during from the detection of the current limit to OFF of P-channel MOS driver transistor.
    ③Because of no potential difference at both ends of the coil, the time rate of coil current becomes quite small.
    ④Lx oscillates very narrow pulses by the current limit for several ms.
    ⑤The circuit is latched, stopping its operation.



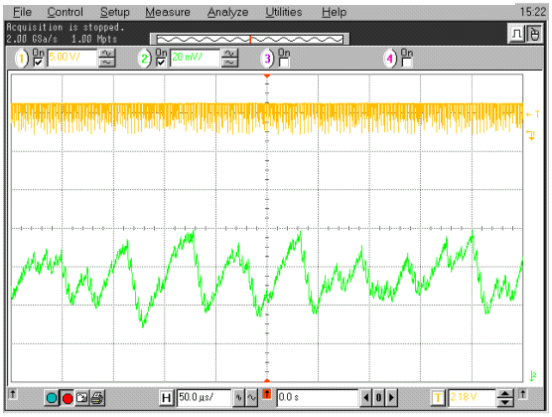
## ■NOTE ON USE (Continued)

13. In order to stabilize $V_{IN2}$ voltage level and oscillation frequency, we recommend that a by-pass capacitor ($C_{IN}$) be connected as close as possible to the $V_{IN2}$ and $V_{SS}$ pins.
14. High step-down ratio and very light load may lead an intermittent oscillation.
15. During PWM / PFM automatic switching mode, operating may become unstable at transition to continuous mode. Please verify with actual design.

$V_{OUT3}$=3.3V, $f_{OSC}$=1.2MHz
$V_{IN2}$=3.7V, $I_{OUT3}$=100mA

CH1:Lx 5V/div

CH2:$V_{OUT3}$ 20mV/div



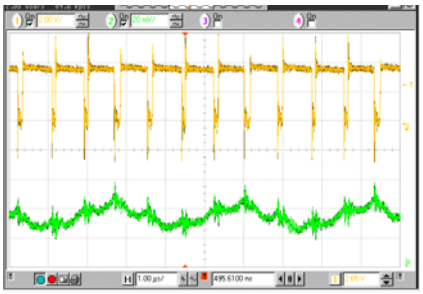

<External Components>
L : 4.7 µ F(NR4018)
$C_{IN2}$ : 4.7 µ F(Ceramic)
$C_{L3}$ : 10 µ F(Ceramic)

16. Please note the inductance value of the coil. The IC may enter unstable operation if the combination of ambient temperature, output voltage, oscillation frequency, and L value are not adequate.
In the operation range close to the maximum duty cycle, The IC may happen to enter unstable output voltage operation even if using the L values listed below.

$V_{OUT3}$=3.3V, $f_{OSC}$=1.2MHz
$V_{IN2}$=4.0V,$I_{OUT3}$=180mA

CH1:Lx 2.0V/div

CH2:$V_{OUT3}$ 20mV/div



<External Components>
L : 1.5 µ F(NR3015)
$C_{IN2}$ : 4.7 µ F(Ceramic)
$C_{L3}$ : 10 µ F(Ceramic)

●The Range of L Value

| $f_{OSC}$ | $V_{OUT}$ | L Value |
|---|---|---|
| 3.0MHz | 0.8V＜$V_{OUT3}$≦4.0V | 1.0 µ H～2.2 µ H |
| 1.2MHz | $V_{OUT3}$≦2.5V | 3.3 µ H～6.8 µ H |
| | 2.5V＜$V_{OUT3}$ | 4.7 µ H～6.8 µ H |

*When a coil less value of 4.7 µ H is used at $f_{OSC}$=1.2MHz or when a coil less value of 1.5 µ H is used at $f_{OSC}$=3.0MHz, peak coil current more easily reach the current limit $I_{LMI}$. In this case, it may happen that the IC can not provide 600mA output current.

## ■NOTE ON USE (Continued)

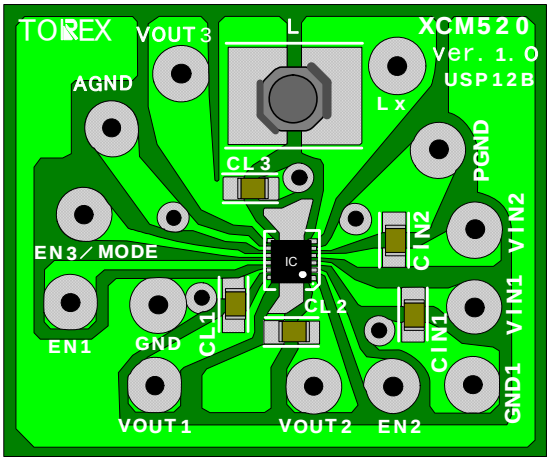
●Note on use of pattern layouts

1. Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. The capacitor ($C_{IN}$) should be connected as close as possible to the $V_{IN}$ and $V_{SS}$ pins.
   When wiring impedance is high, noise propagation by output current or phase discrepancy occur which results in unstable operating. In this case, please reinforce $V_{IN}$ and $V_{SS}$ rails. If the operation is still unstable, please increase input capacitance $C_{IN}$.
3. With comparison to the separate product usage, the two chips are placed in adjacent in the package so heat generation Is influenced each other. Please evaluate and verify in the actual design.

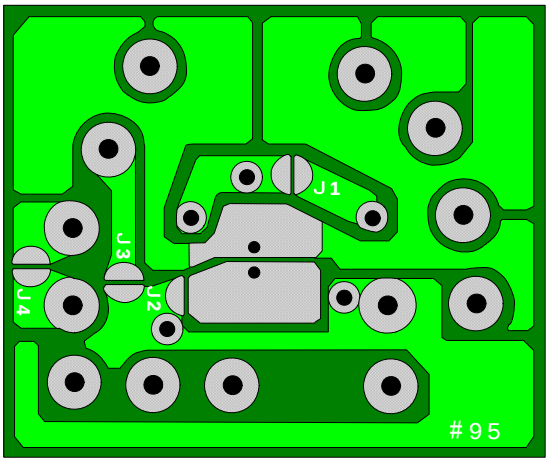
●Instructions of pattern layouts

1. In order to stabilize $V_{IN1}$・$V_{IN2}$・$V_{OUT1}$・$V_{OUT2}$・$V_{OUT3}$, we recommend that a by-pass capacitor ($C_{IN1}$・$C_{IN2}$・$C_{L1}$・$C_{L2}$・$C_{L3}$) be connected as close as possible to the $V_{IN1}$・$V_{IN2}$・$V_{OUT1}$・$V_{OUT2}$・$V_{OUT3}$ and $V_{SS}$ pin.
2. Please mount each external component as close to the IC as possible.
3. Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
4. $V_{SS}$（AGND・PGND・$V_{SS}$）ground wiring is recommended to get large area. The IC may goes into unstable operation as a result of $V_{SS}$ voltage level fluctuation during the switching.
5. Heat is generated because of the output current ($I_{OUT}$) and ON resistance of driver transistors.

●Reference Pattern Layout




Front



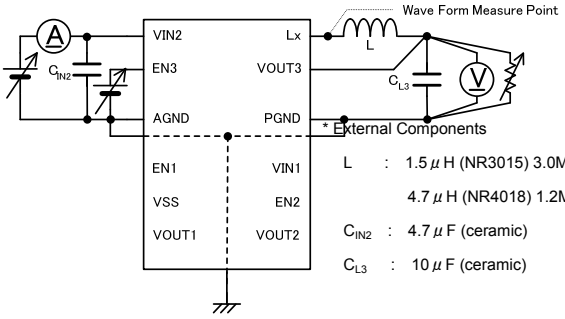

Back

Ceramic Capacitor

Inductor

# ■TEST CIRCUITS

〈 Circuit No.1 〉



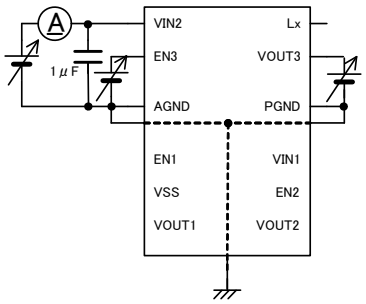

* External Components

L : 1.5 μH (NR3015) 3.0MHz
4.7 μH (NR4018) 1.2MHz

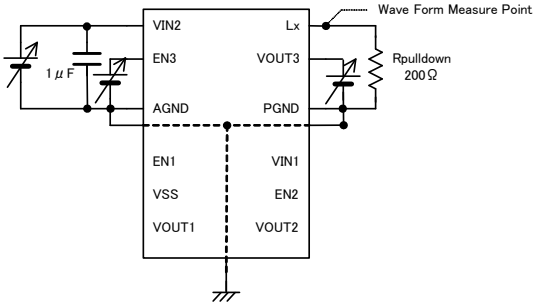
$C_{IN2}$ : 4.7 μF (ceramic)

$C_{L3}$ : 10 μF (ceramic)

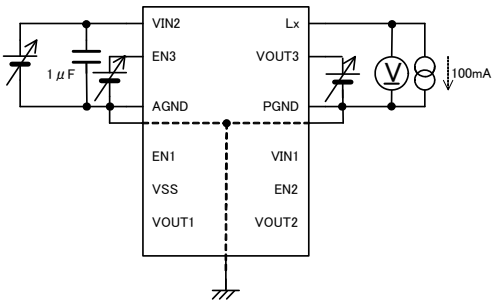
〈 Circuit No.2 〉



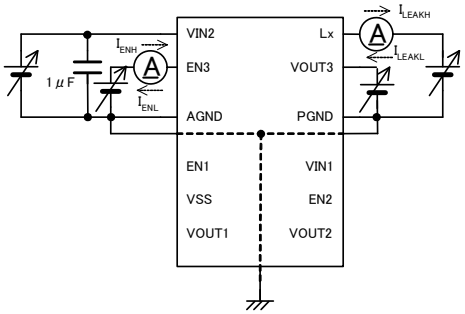

〈 Circuit No.3 〉



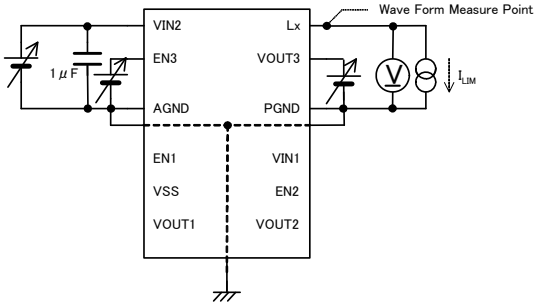

〈 Circuit No.4 〉



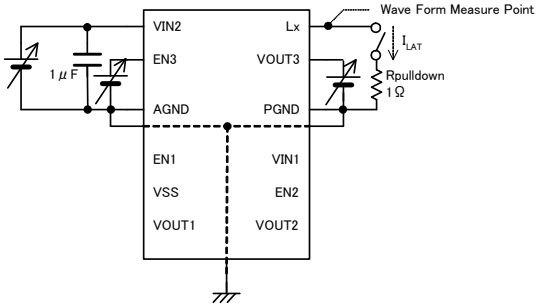

〈 Circuit No.5 〉



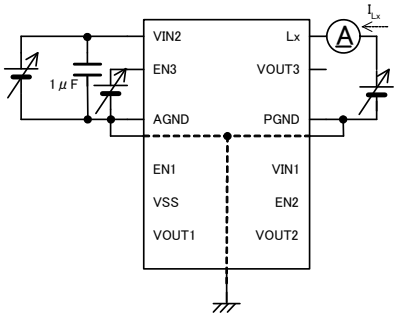

〈 Circuit No.6 〉



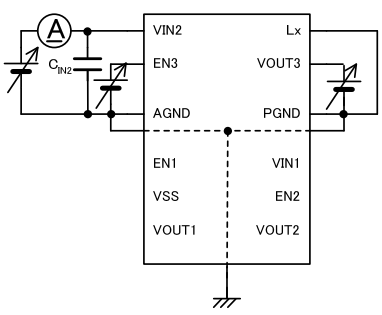

〈 Circuit No.7 〉




〈 Circuit No.8 〉




〈 Circuit No.9 〉



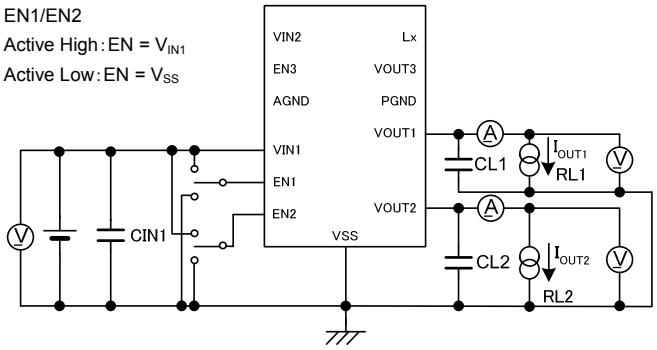
## ■TEST CIRCUITS (Continued)

〈 Circuit No10 〉

EN1/EN2

Active High : EN = $V_{IN1}$

Active Low : EN = $V_{SS}$



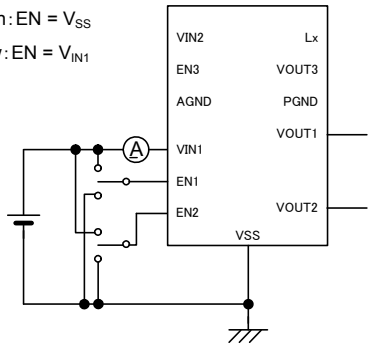

$C_{IN1}$, $C_{L1}$, $C_{L2}$ : 1 μF (ceramic)

〈 Circuit No11 〉

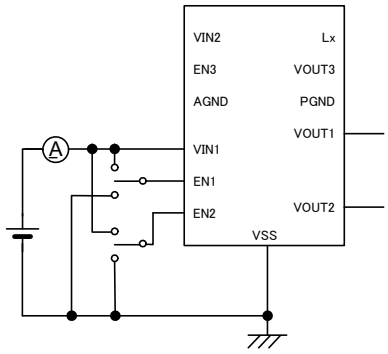
EN1/EN2

Active High : EN = $V_{SS}$

Active Low : EN = $V_{IN1}$




〈 Circuit No12 〉




EN1/EN2

Active High (pull-down, without resistance)

VR1 Supply Current, EN1=ON, EN2=OFF

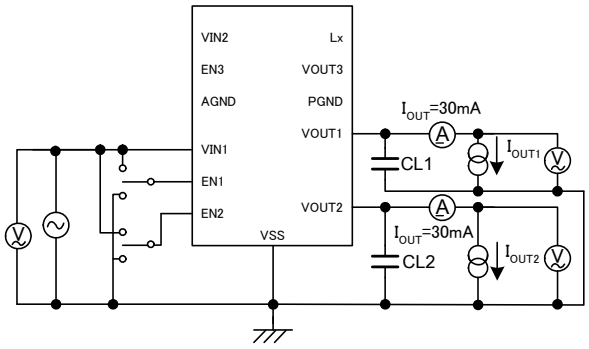
VR2 Supply Current, EN1= OFF, EN2=ON

Active High: ON=$V_{IN1}$, OFF=$V_{SS}$

Active Low: ON=$V_{SS}$, OFF=$V_{IN1}$

〈 Circuit No13 〉

$V_{IN1}$=[$V_{OUT}$(T)+1.0]VDC+0.5Vp-pAC




$C_{L1}$, $C_{L2}$ : 1 μF (ceramic)

EN1/EN2

VR1 PSRR

EN1=ON, EN2=OFF

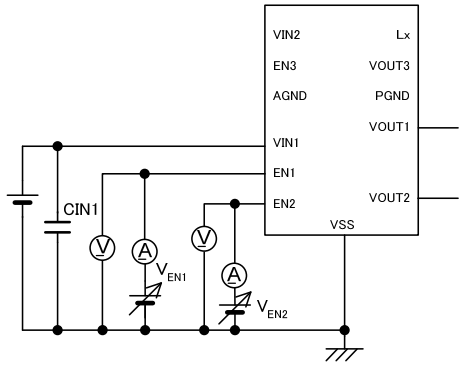
VR2 PSRR

EN1=OFF, EN2=ON

Active High: ON=$V_{IN1}$, OFF=$V_{SS}$

Active Low: ON=$V_{SS}$, OFF=$V_{IN1}$

〈 Circuit No14 〉




$C_{IN1}$ : 1 μF (ceramic)

EN1/EN2

EN1"H" Level Current

EN1=$V_{IN1}$ Level

EN2"H" Level Current

EN2=$V_{IN1}$ Level

EN1"L" Level Current

EN1= $V_{SS}$

EN2"L" Level Current

EN2=$V_{SS}$

* The EN which is not measured is in operation sop mode.

Active High: $V_{SS}$

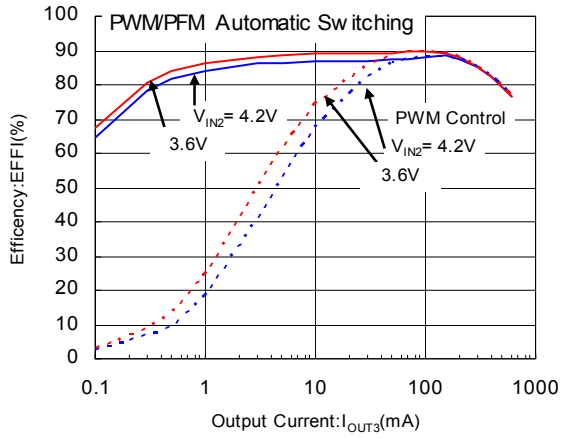
Active Low: measuring $V_{IN1}$ Level

# ■TYPICAL PERFORMANCE CHARACTERISTICS

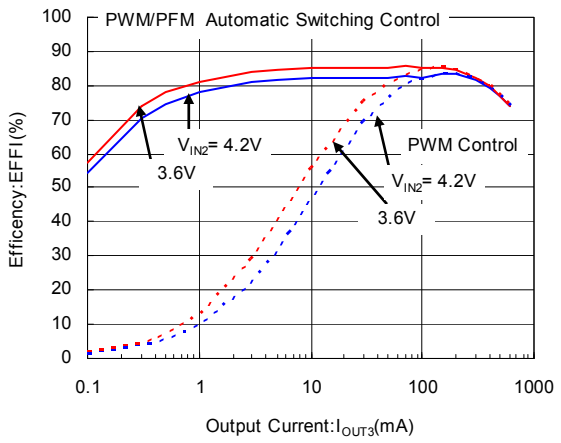
## ●DC/DC Block

### (1) Efficiency vs. Output Current

$V_{OUT3}$=1.8V, $f_{OSC}$=1.2MHz
L=4.7μH(NR4018), $C_{IN2}$=4.7μF, $C_{L3}$=10μF

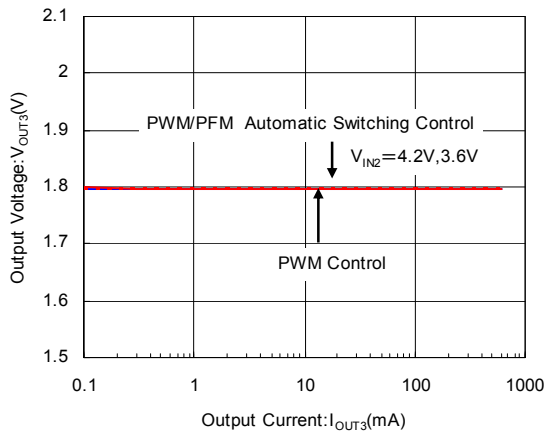



$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz
L=1.5μH(NR3015), $C_{IN2}$=4.7μF, $C_{L3}$=10μF

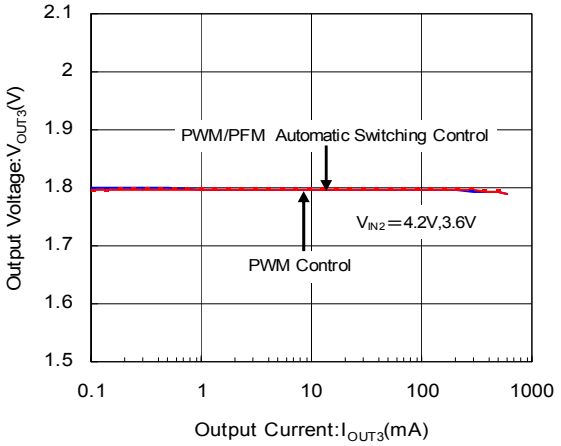



### (2) Output Voltage vs. Output Current

$V_{OUT3}$=1.8V, $f_{OSC}$=1.2MHz
L=4.7μH(NR4018), $C_{IN2}$=4.7μF, $C_{L3}$=10μF

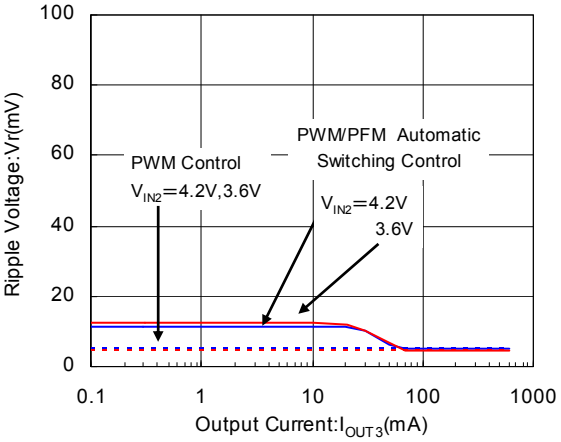



$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz
L=1.5μH(NR3015), $C_{IN2}$=4.7μF, $C_{L3}$=10μF

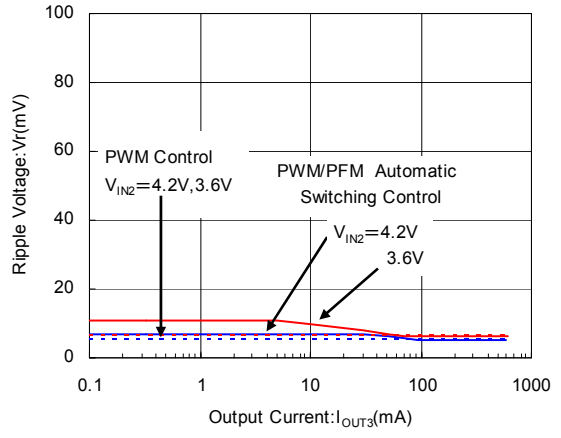



### (3) Ripple Voltage vs. Output Current

$V_{OUT3}$=1.8V, $f_{OSC}$=1.2MHz
L=4.7μH(NR4018), $C_{IN2}$=4.7μF, $C_{L3}$=10μF




$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz
L=1.5μH(NR3015), $C_{IN2}$=4.7μF, $C_{L3}$=10μF



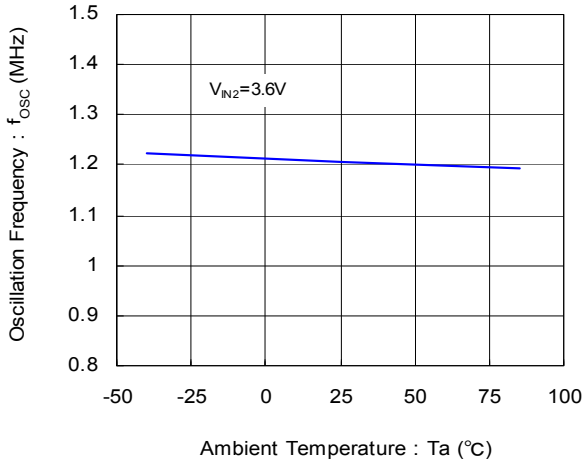
## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●DCDC Block (Continued)

(4) Oscillation Frequency vs. Ambient Temperature

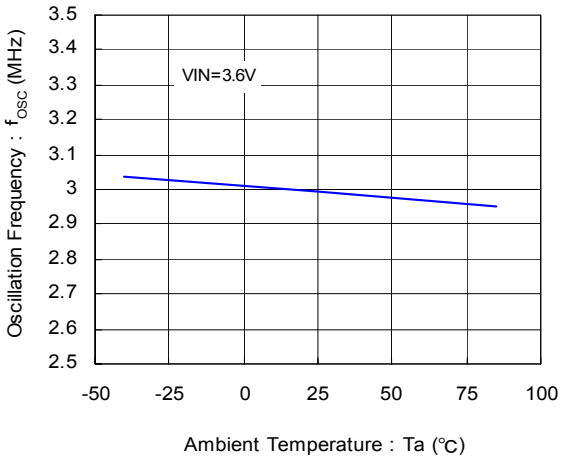
$V_{OUT3}$=1.8V, $f_{OSC}$=1.2MHz

L=4.7μH(NR4018), $C_{IN2}$=4.7μF, $C_{L3}$=10μF



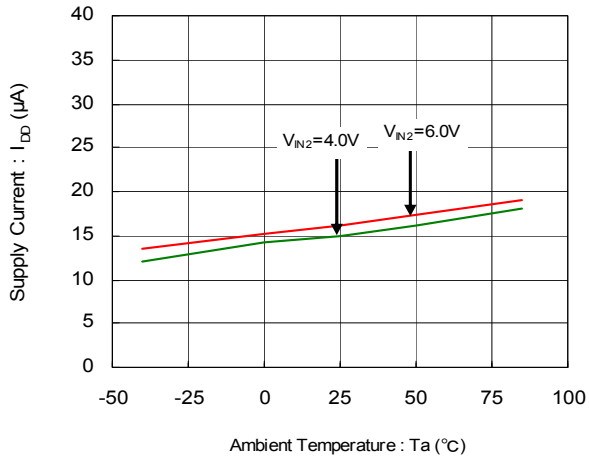

$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz

L=1.5μH(NR3015), $C_{IN2}$=4.7μF, $C_{L3}$=10μF

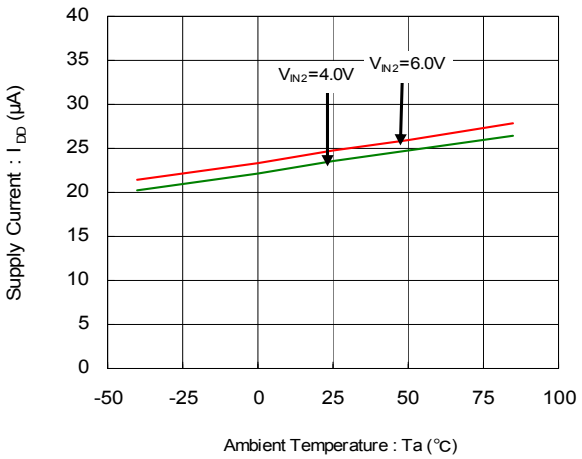



(5) Supply Current vs. Ambient Temperature

$V_{OUT3}$=1.8V, $f_{OSC}$=1.2MHz

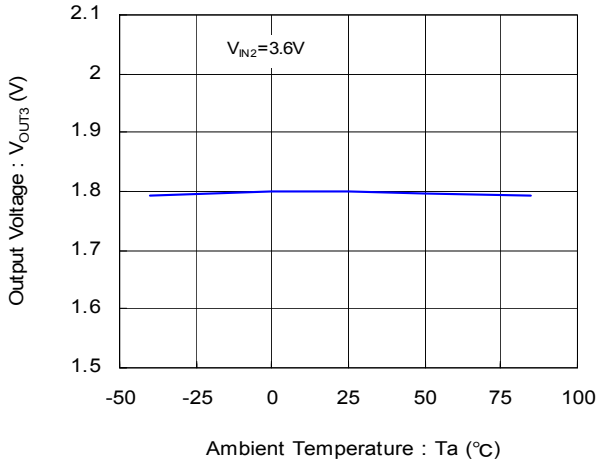



$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz



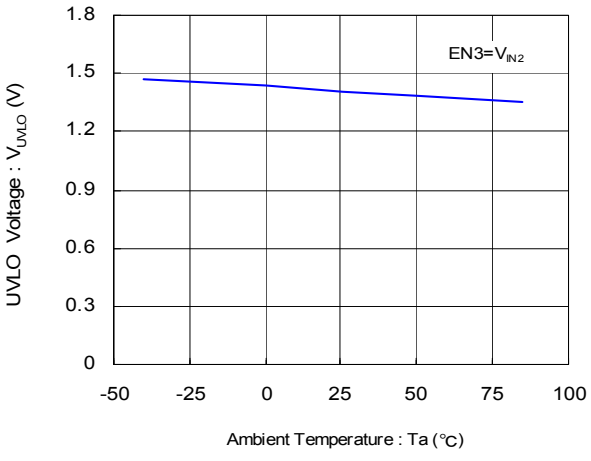

(6) Output Voltage vs. Ambient Temperature

$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz




(7) UVLO Voltage vs. Ambient Temperature

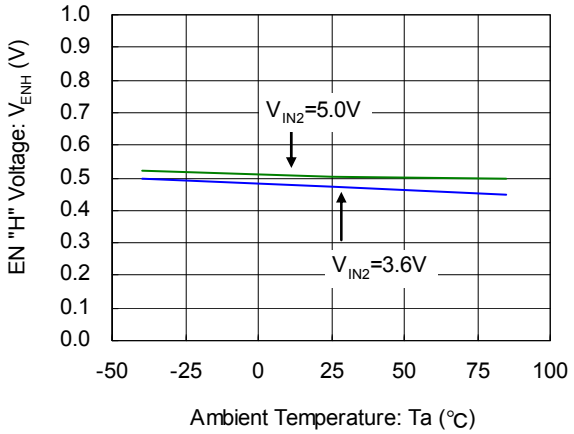
$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz



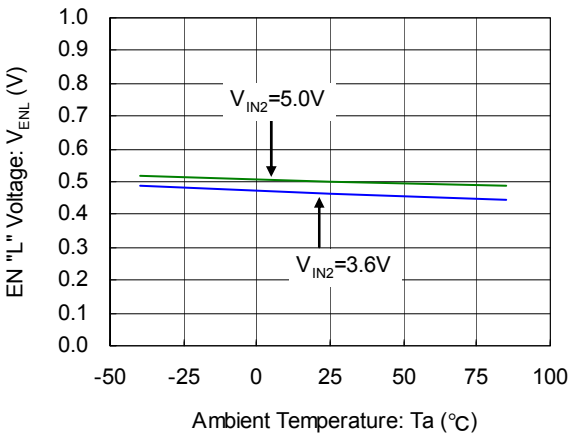
# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●DCDC Block (Continued)

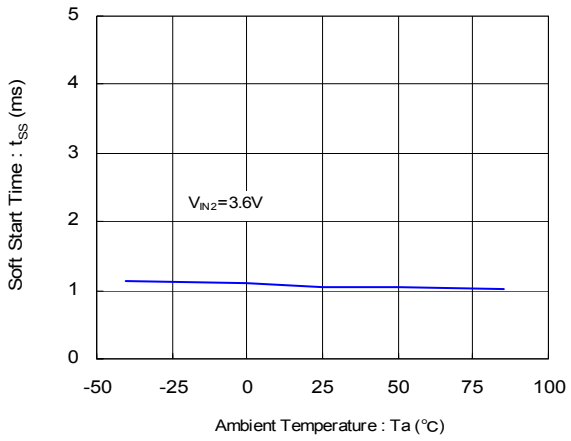
(8) EN "H" Voltage vs. Ambient Temperature
$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz



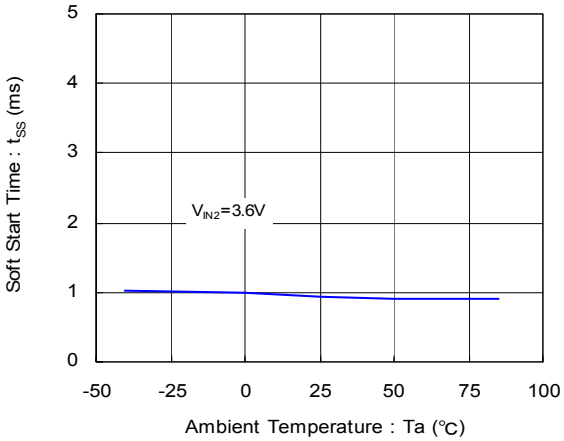

(9) EN" L" Voltage vs. Ambient Temperature
$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz



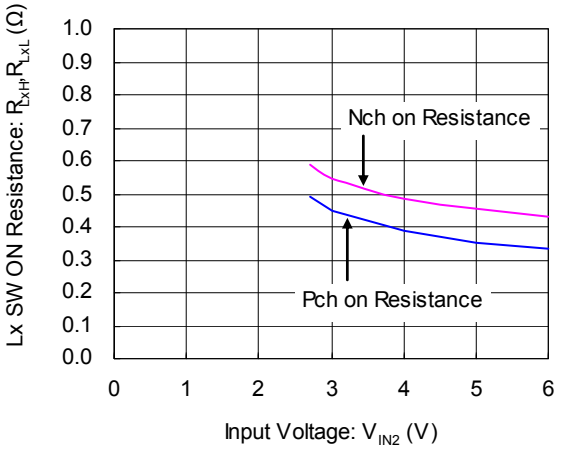

(10) Soft Start Time vs. Ambient Temperature
$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz
L=4.7μH(NR4018), $C_{IN2}$=4.7μF, $C_{L3}$=10μF




$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz
L=1.5μH(NR3015), $C_{IN2}$=4.7μF, $C_{L3}$=10μF




(11) "Pch / Nch" Driver on Resistance vs. Input Voltage
$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz



## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●DCDC Block (Continued)

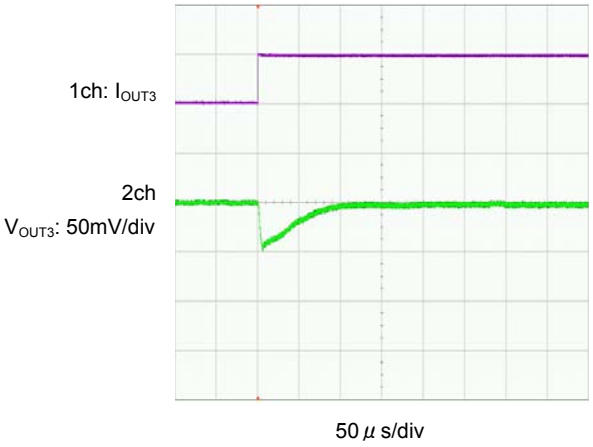
(12) Load Transient Response

$V_{OUT3}$=1.8V, $f_{OSC}$=3.0MHz(PWM Control)

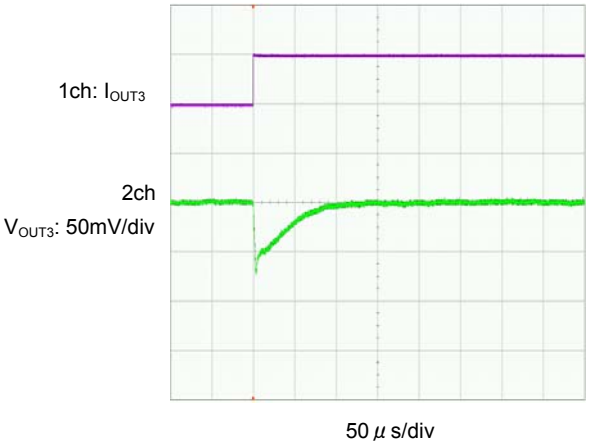
L=1.5μH(NR3015), $C_{IN2}$=4.7μF(ceramic), $C_{L3}$=10μF(ceramic), Topr=25℃

$V_{IN2}$=3.6V, EN1=$V_{IN2}$

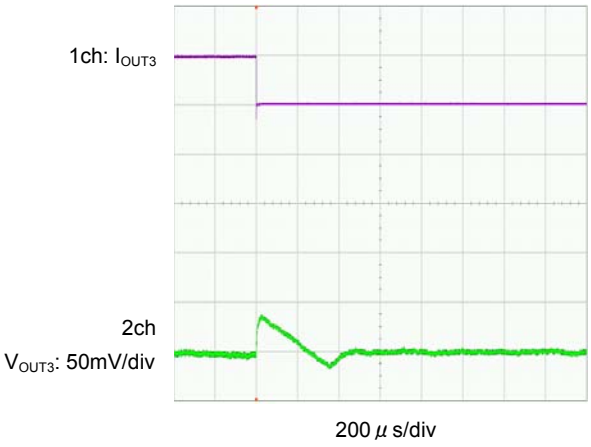
$I_{OUT3}$=1mA → 100mA



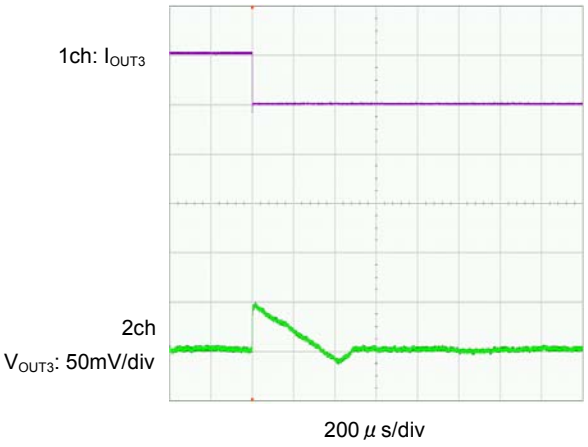

$I_{OUT3}$=1mA → 300mA




$I_{OUT3}$=100mA → 1mA




$I_{OUT3}$=300mA → 1mA



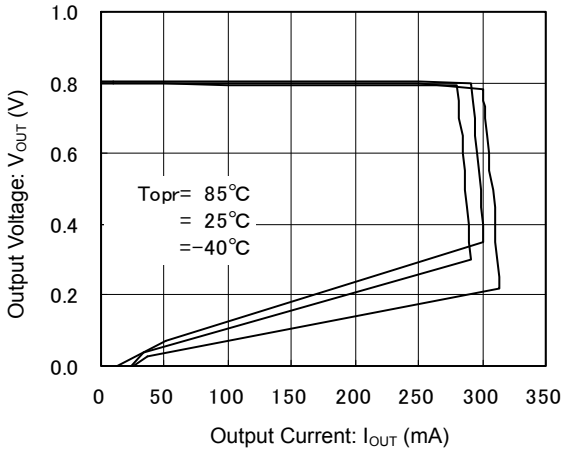
# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

## ●Regulator Block

(1) Output Voltage vs. Output Current

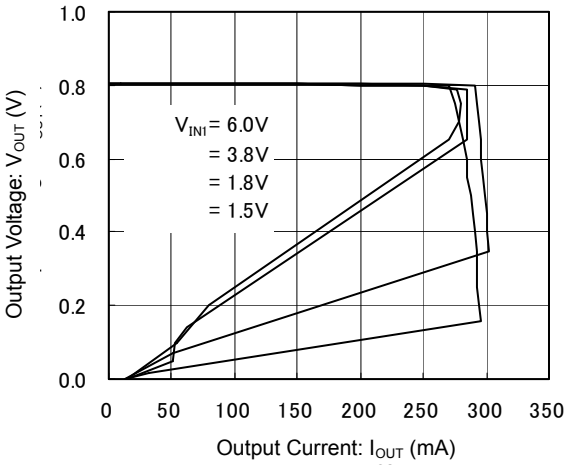
$V_{OUT}$=0.8V

$V_{IN1}$=1.8V, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



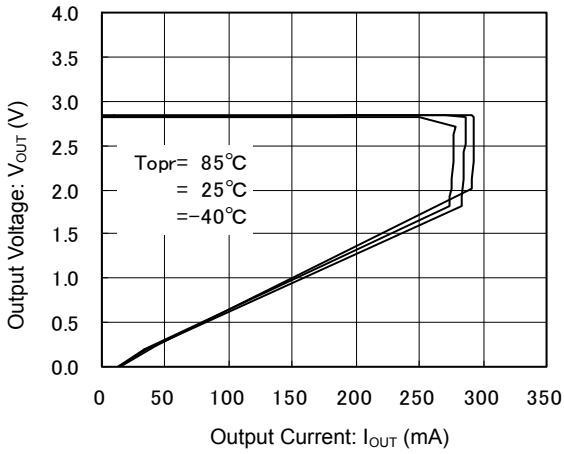

$V_{OUT}$=0.8V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



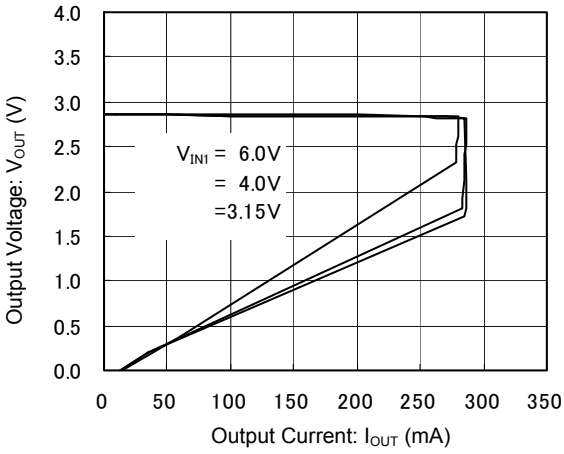

$V_{OUT}$=2.85V

$V_{IN1}$=3.85V, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



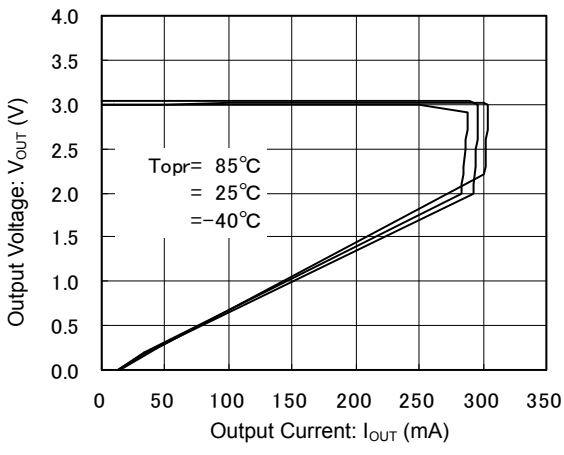

$V_{OUT}$=2.85V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



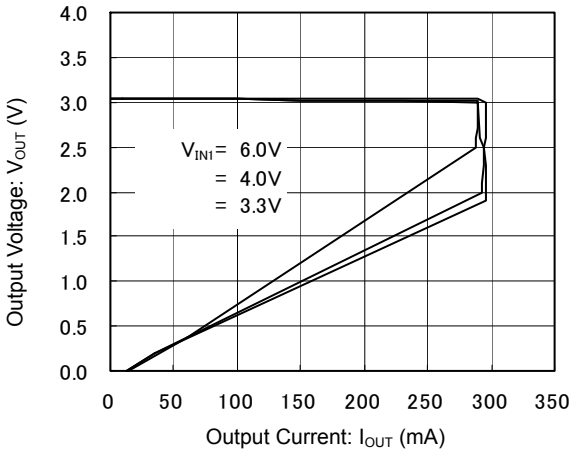

$V_{OUT}$=3.0V

$V_{IN1}$=4.0V, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




$V_{OUT}$=3.0V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



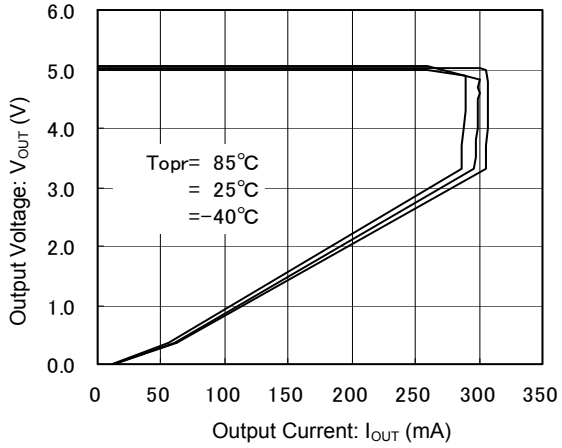
# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●Regulator Block (Continued)

(1) Output Voltage vs. Output Current (Continued)

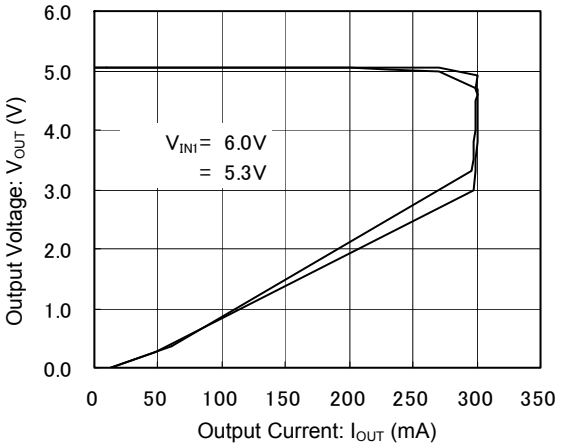
$V_{OUT}$=5.0V

$V_{IN1}$=4.0V, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




$V_{OUT}$=5.0V

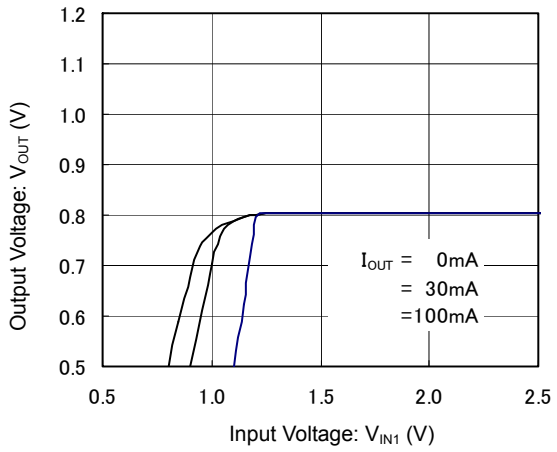
Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




(2) Output Voltage vs. Input Voltage

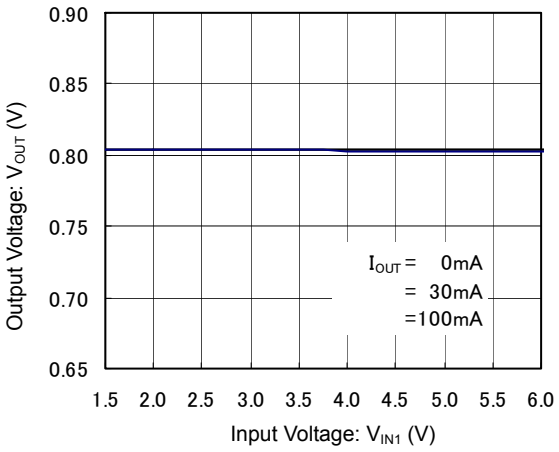
$V_{OUT}$=0.8V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



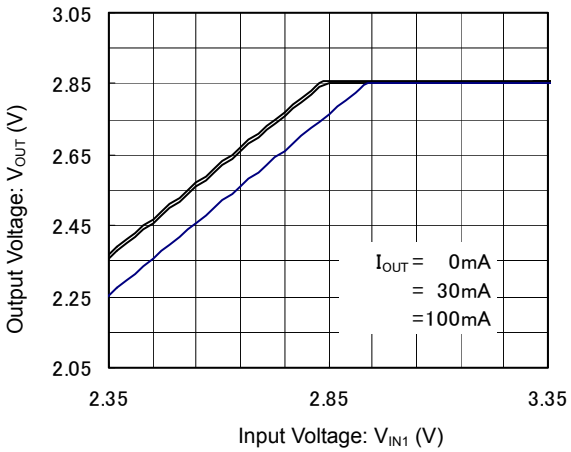

$V_{OUT}$=0.8V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



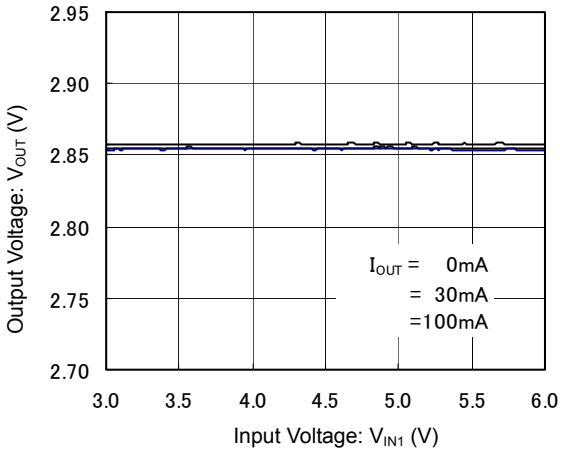

$V_{OUT}$=2.85V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




$V_{OUT}$=2.85V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



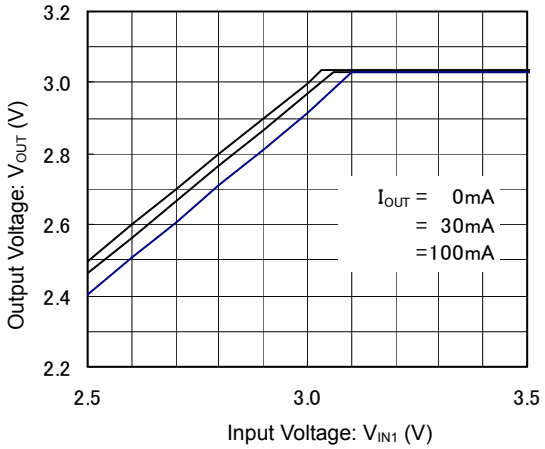
# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

## ●Regulator Block (Continued)

(2) Output Voltage vs. Input Voltage (Continued)

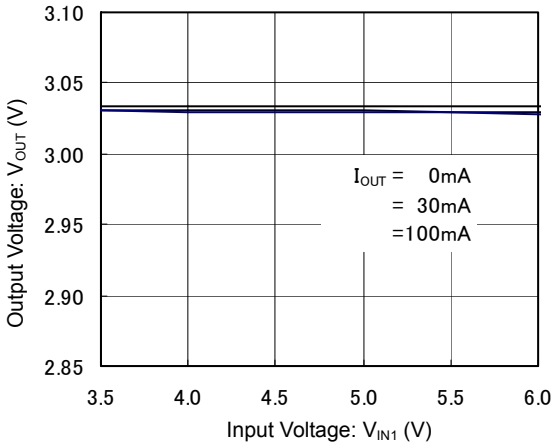
$V_{OUT}$=3.0V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



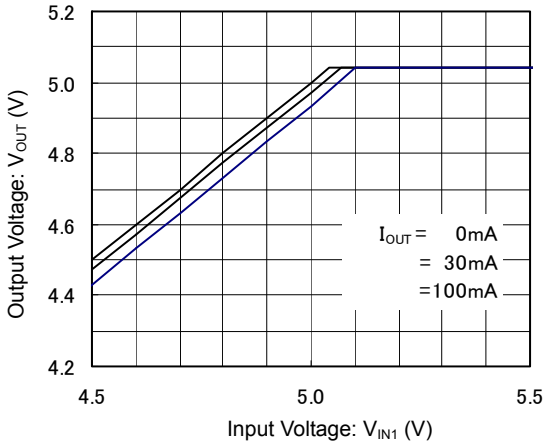

$V_{OUT}$=3.0V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



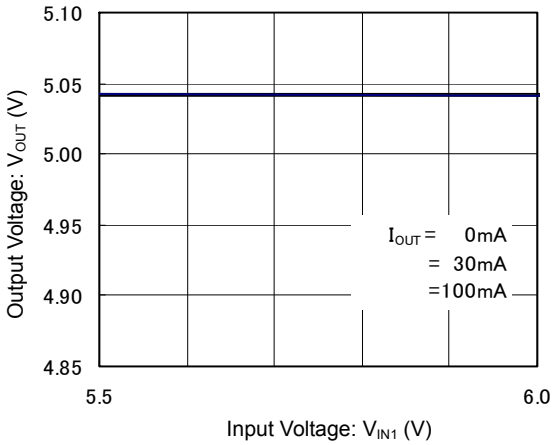

$V_{OUT}$=5.0V

Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




$V_{OUT}$=5.0V

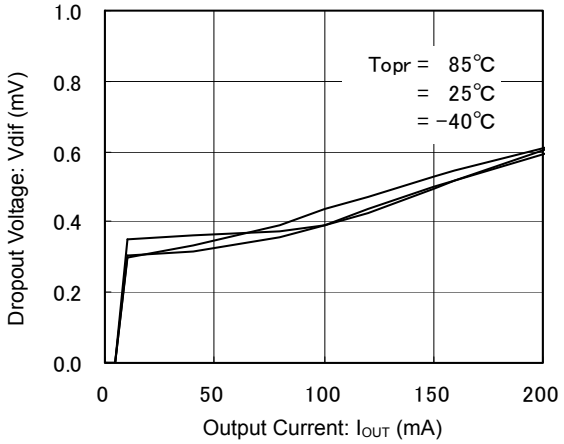
Ta=25℃, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




(3) Dropout Voltage vs. Output Current

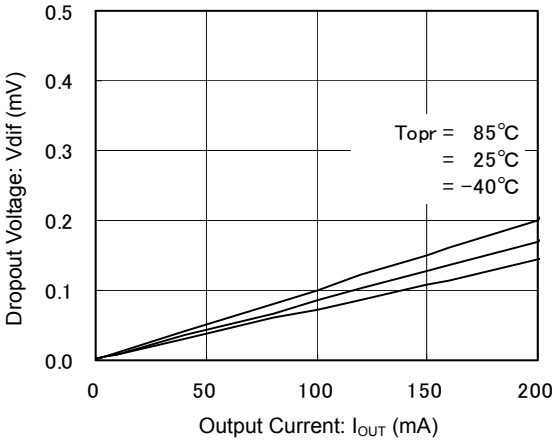
$V_{OUT}$=0.8V

$C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




$V_{OUT}$=2.85V

$C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



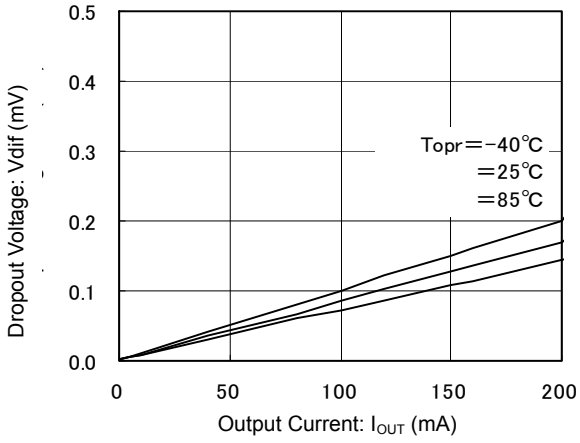
## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●Regulator Block (Continued)

(3) Dropout Voltage vs. Output Current (Continued)

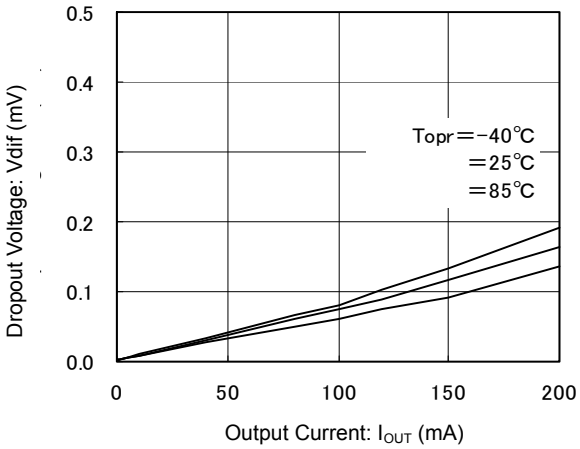
$V_{OUT}$=3.0V

$C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



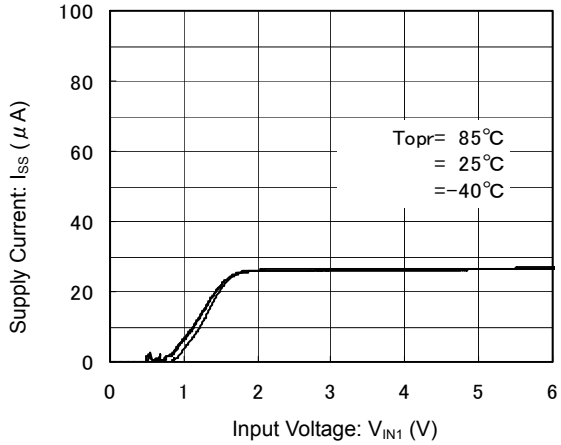

$V_{OUT}$=5.0V

$C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)

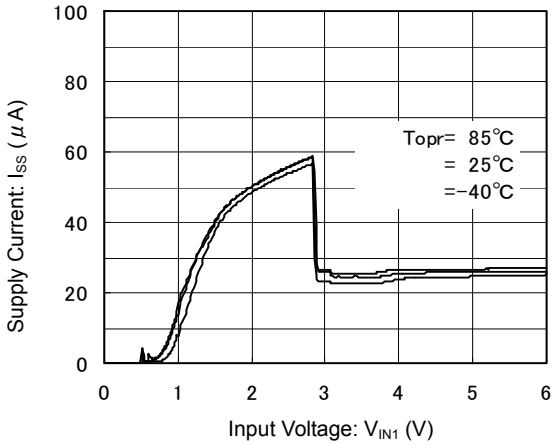



(4) Supply Current vs. Input Voltage

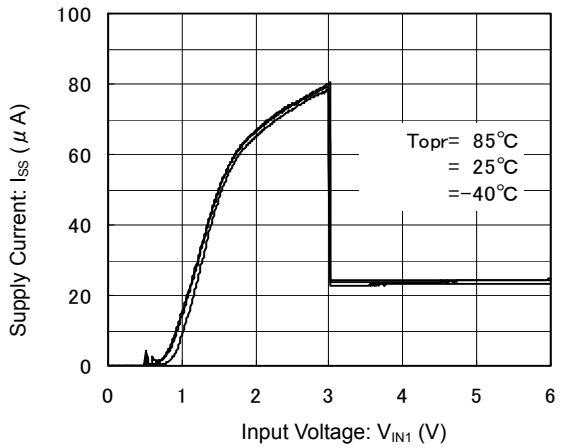
$V_{OUT}$=0.8V



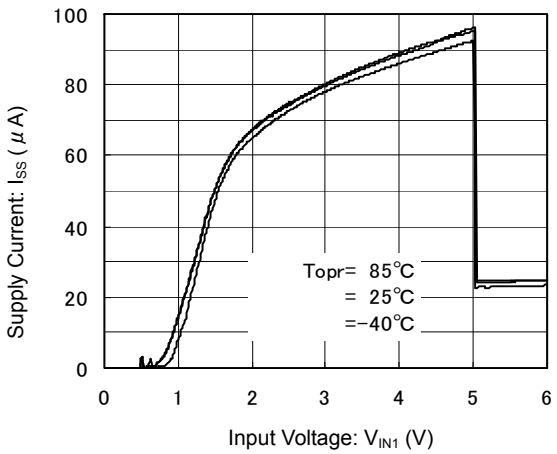

$V_{OUT}$=2.85V




$V_{OUT}$=3.0V




$V_{OUT}$=5.0V



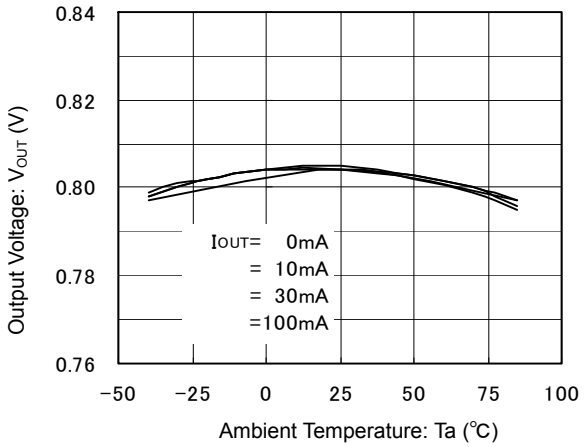
# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

## ●Regulator Block (Continued)

(5) Output Voltage vs. Ambient Temperature

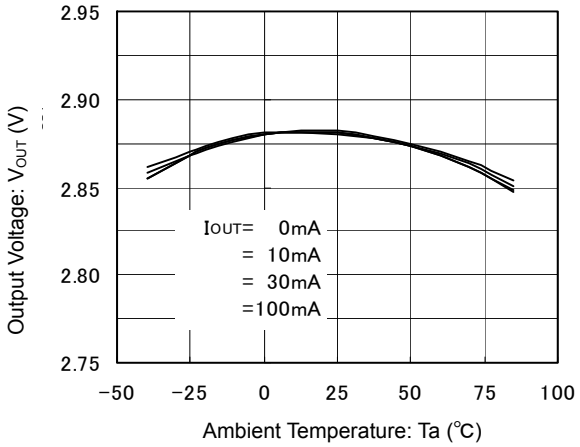
$V_{OUT}$=0.8V

$V_{IN1}$=1.8V, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



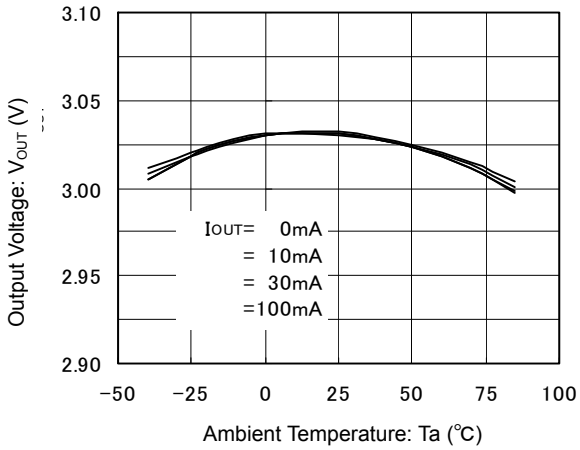

$V_{OUT}$=2.85V

$V_{IN1}$=4.0V, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)



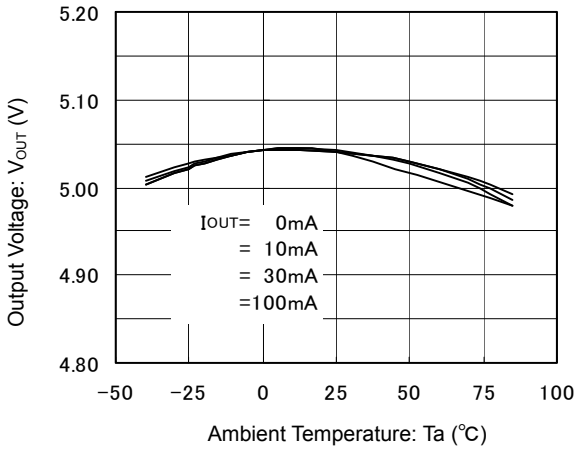

$V_{OUT}$=3.0V

$V_{IN1}$=4.0V, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




$V_{OUT}$=5.0V

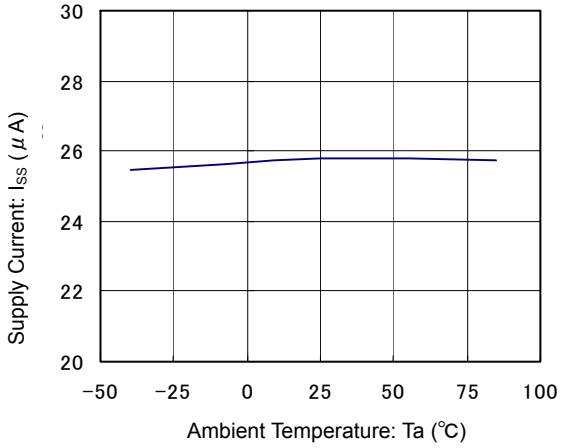
$V_{IN1}$=6.0V, $C_{IN1}$=1μF(ceramic), $C_L$=1μF(ceramic)




(6) Supply Current vs. Ambient Temperature

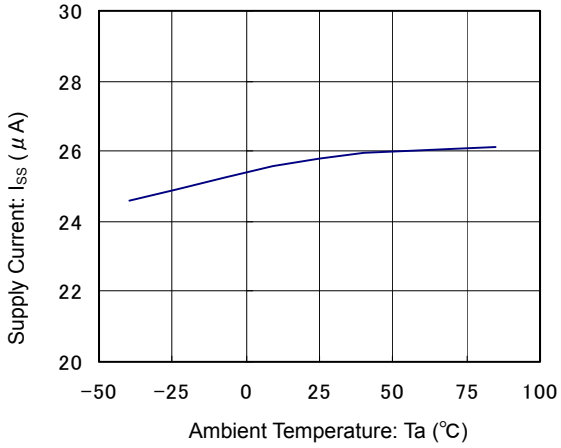
$V_{OUT}$=0.8V

$V_{IN1}$=1.8V




$V_{OUT}$=2.85V

$V_{IN1}$=3.85V



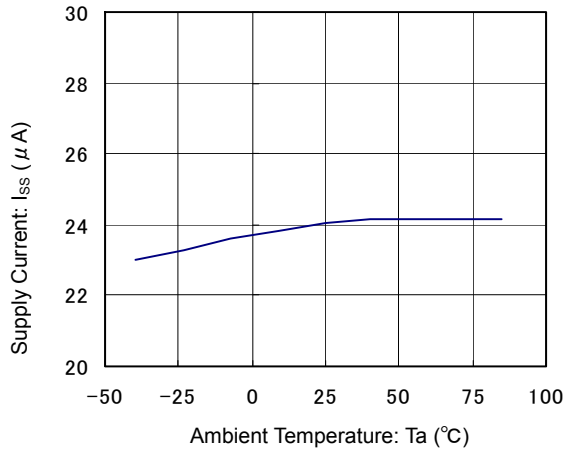
## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

### ●Regulator Block (Continued)

(6) Supply Current vs. Ambient Temperature (Continued)

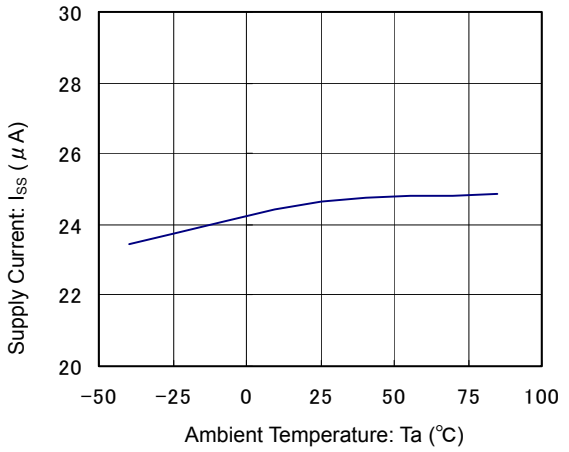
$V_{OUT}$=3.0V

$V_{IN1}$=4.0V




$V_{OUT}$=5.0V

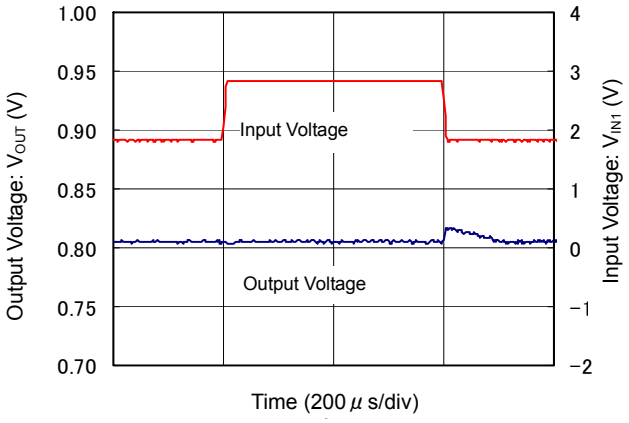
$V_{IN1}$=6.0V




(7) Input Transient Response

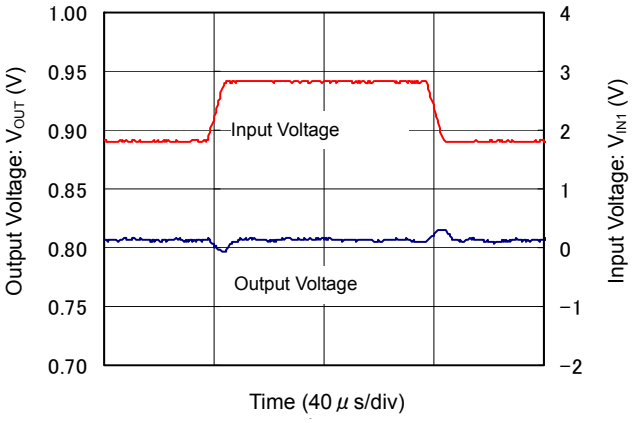
$V_{OUT}$=0.8V

tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=100μA



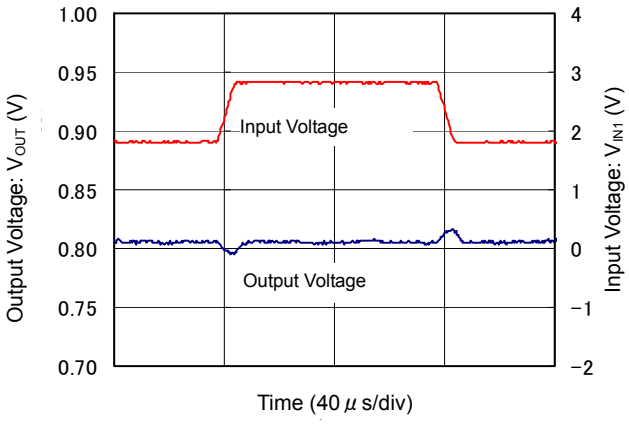

$V_{OUT}$=0.8V

tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=30mA



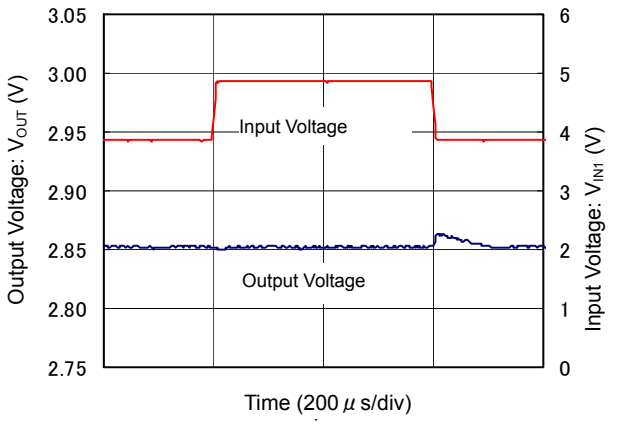

$V_{OUT}$=0.8V

tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=100mA




$V_{OUT}$=2.85V

tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=100μA

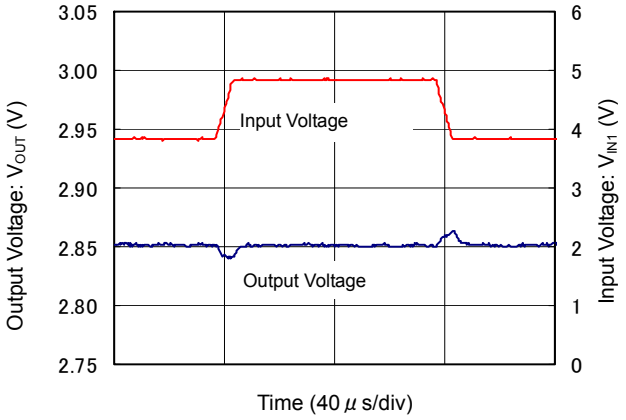


# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

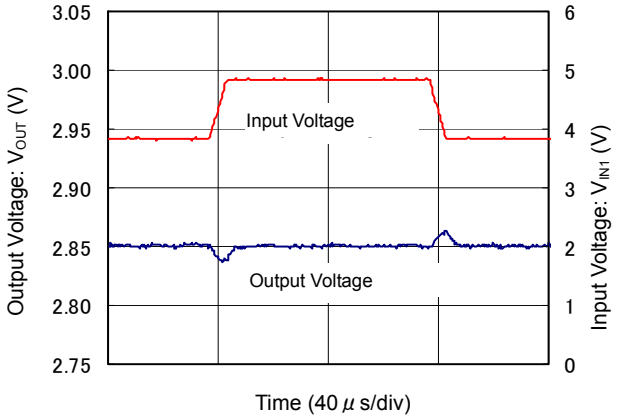
## ●Regulator Block (Continued)

### (7) Input Transient Response (Continued)

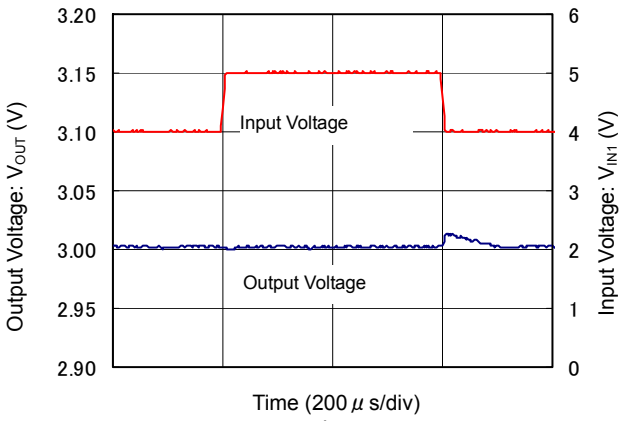
$V_{OUT}$=2.85V
tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=30mA



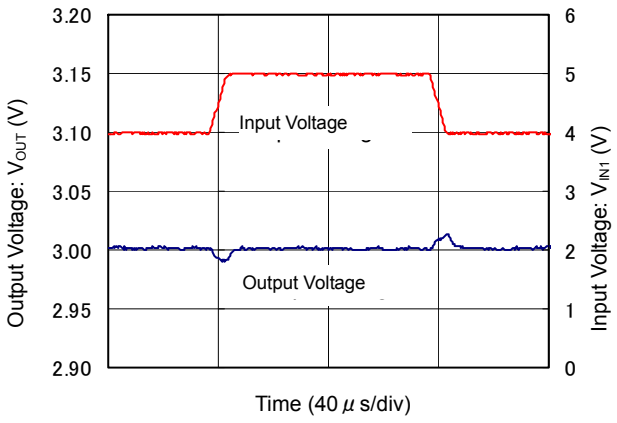

$V_{OUT}$=2.85V
tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=100mA



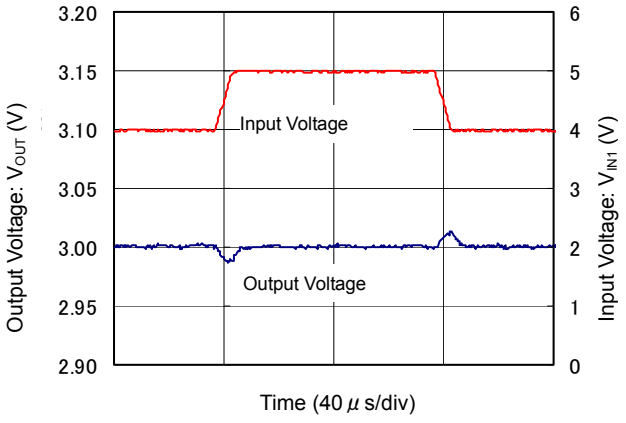

$V_{OUT}$=3.0V
tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=100μA



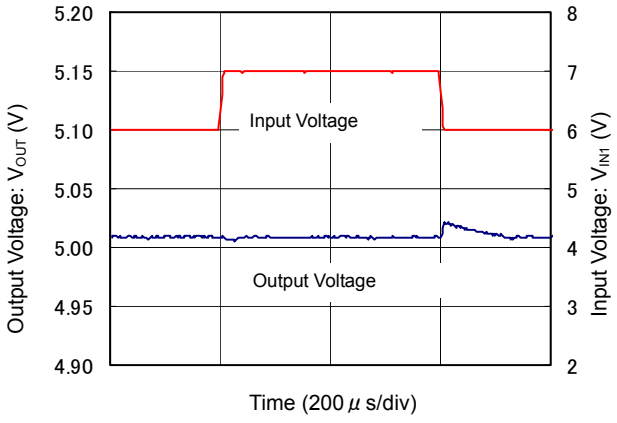

$V_{OUT}$=3.0V
tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=30mA




$V_{OUT}$=3.0V
tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=100mA




$V_{OUT}$=5.0V
tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=100μA



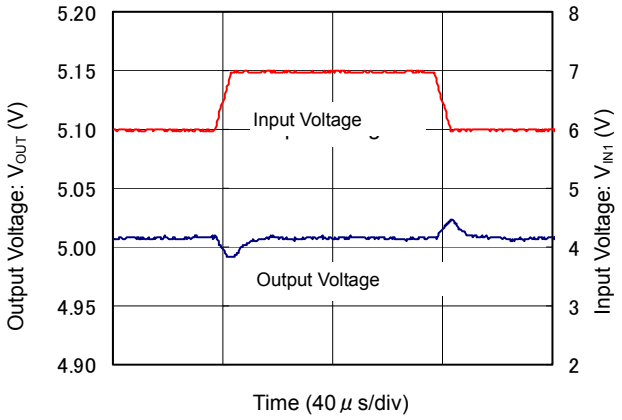
## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●Regulator Block (Continued)

(7) Input Transient Response (Continued)

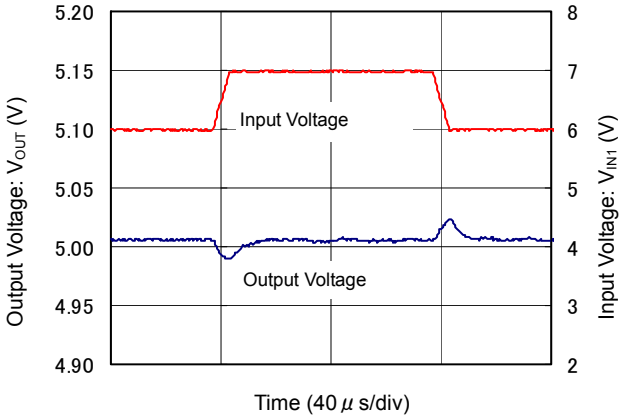
$V_{OUT}$=5.0V

tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=30mA




$V_{OUT}$=5.0V

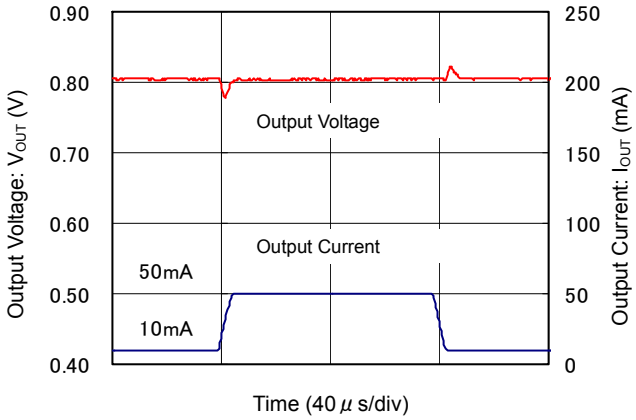
tr=tf=5μs, $C_L$=1μF(ceramic), $I_{OUT}$=100mA




(8) Load Transient Response

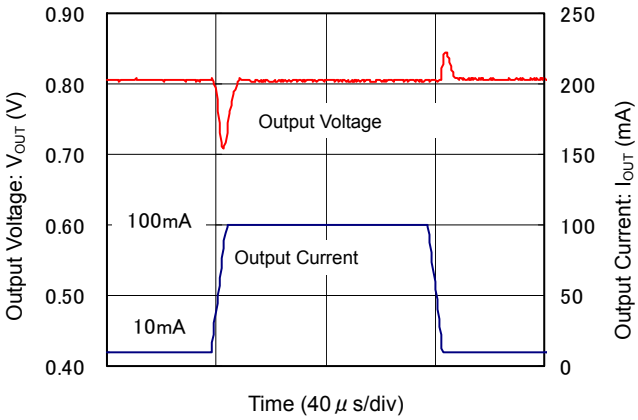
$V_{OUT}$=0.8V

$V_{IN1}$=1.8V, tr=tf=5μs, $C_{IN1}$=$C_L$=1μF(ceramic)



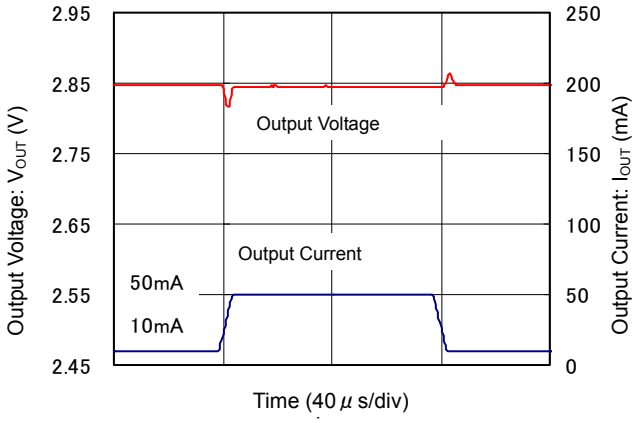

$V_{OUT}$=0.8V

$V_{IN1}$=1.8V, tr=tf=5μs, $C_{IN1}$=$C_L$=1μF(ceramic)



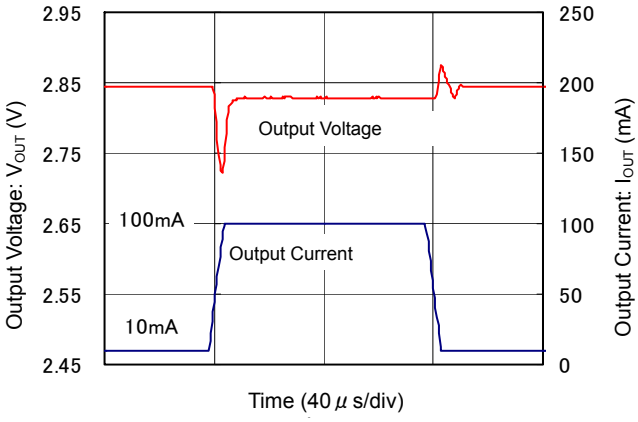

$V_{OUT}$=2.85V

$V_{IN1}$=4.0V, tr=tf=5μs, $C_{IN1}$=$C_L$=1μF(ceramic)




$V_{OUT}$=2.85V

$V_{IN1}$=4.0V, tr=tf=5μs, $C_{IN1}$=$C_L$=1μF(ceramic)

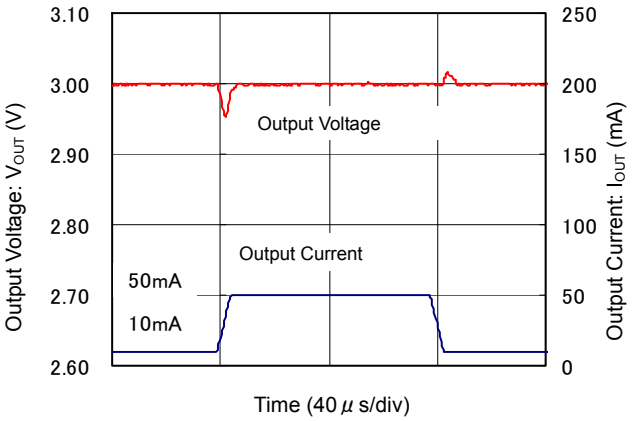


# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

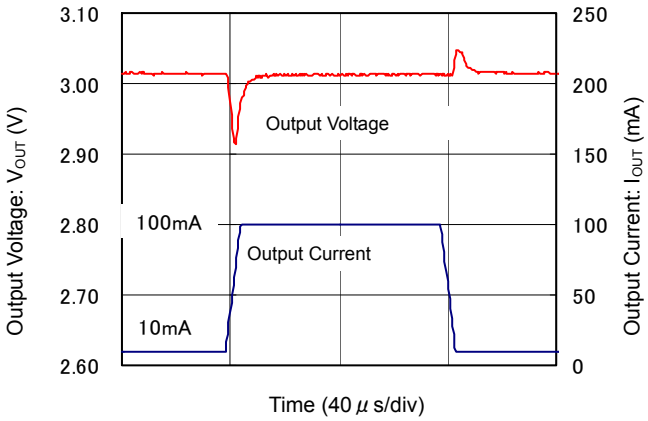
## ●Regulator Block (Continued)

### (8) Load Transient Response (Continued)

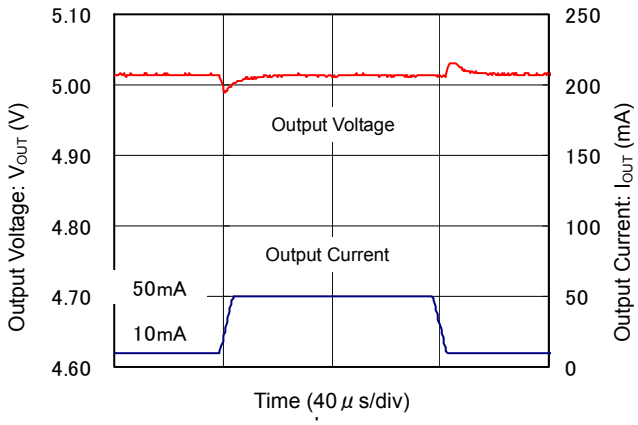
$V_{OUT}$=3.0V
$V_{IN1}$=4.0V, tr=tf=5μs, $C_{IN1}$=$C_L$=1μF(ceramic)



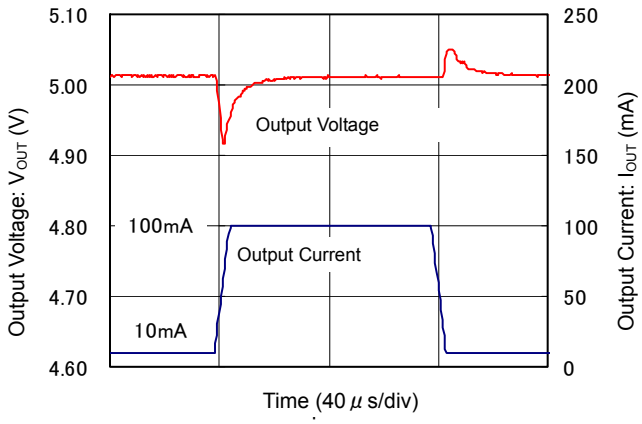

$V_{OUT}$=3.0V
$V_{IN1}$=4.0V, tr=tf=5μs, $C_{IN1}$=$C_L$=1μF(ceramic)




$V_{OUT}$=5.0V
$V_{IN1}$=6.0V, tr=tf=5μs, $C_{IN1}$=$C_L$=1μF(ceramic)

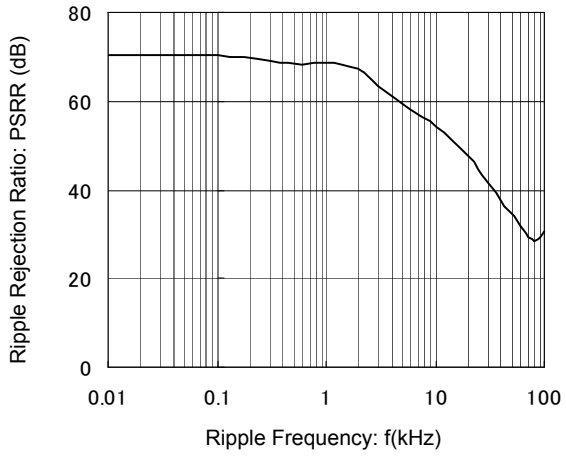



$V_{OUT}$=5.0V
$V_{IN1}$=6.0V, tr=tf=5μs, $C_{IN1}$=$C_L$=1μF(ceramic)

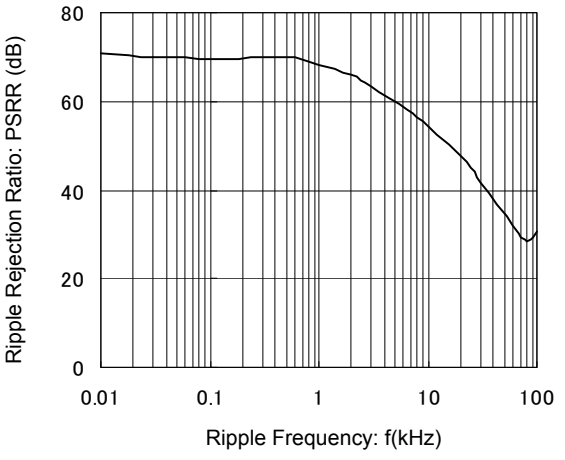



### (9) Ripple Rejection Rate

$V_{OUT}$=0.8V
$V_{IN1}$=1.8VDC+0.5Vp-pAC, $I_{OUT}$=30mA, $C_L$=1μF(ceramic)




$V_{OUT}$=2.85V
$V_{IN1}$=3.85VDC+0.5Vp-pAC, $I_{OUT}$=30mA, $C_L$=1μF(ceramic)



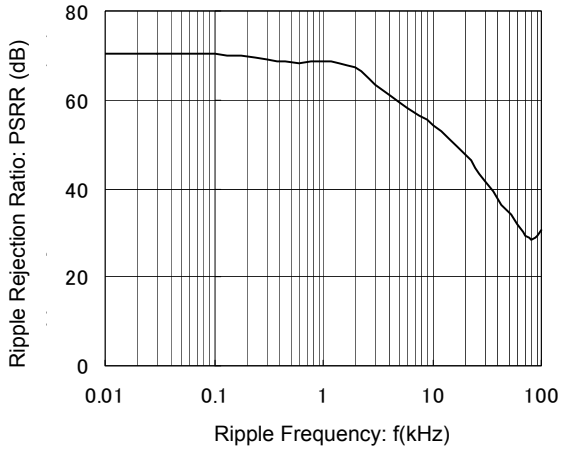
## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

●Regulator Block (Continued)

(9) Ripple Rejection Rate (Continued)

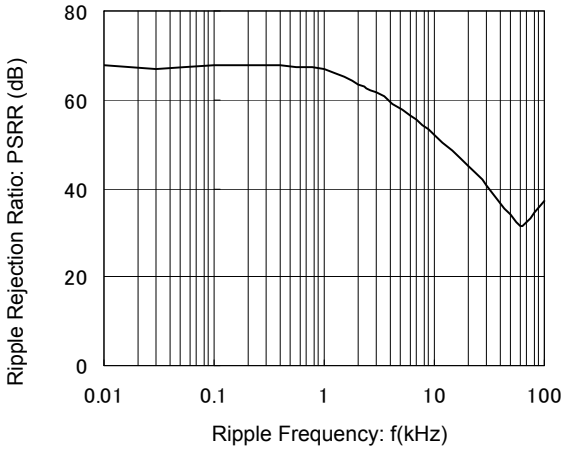
$V_{OUT}$=3.0V

$V_{IN1}$=4.0VDC+0.5Vp-pAC, $I_{OUT}$=30mA, $C_L$=1 μF(ceramic)




$V_{OUT}$=5.0V

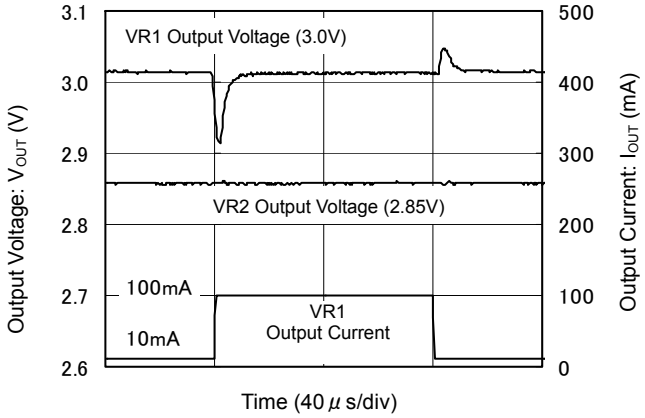
$V_{IN1}$=5.75VDC+0.5Vp-pAC, $I_{OUT}$=30mA, $C_L$=1 μF(ceramic)




(10) Cross Talk

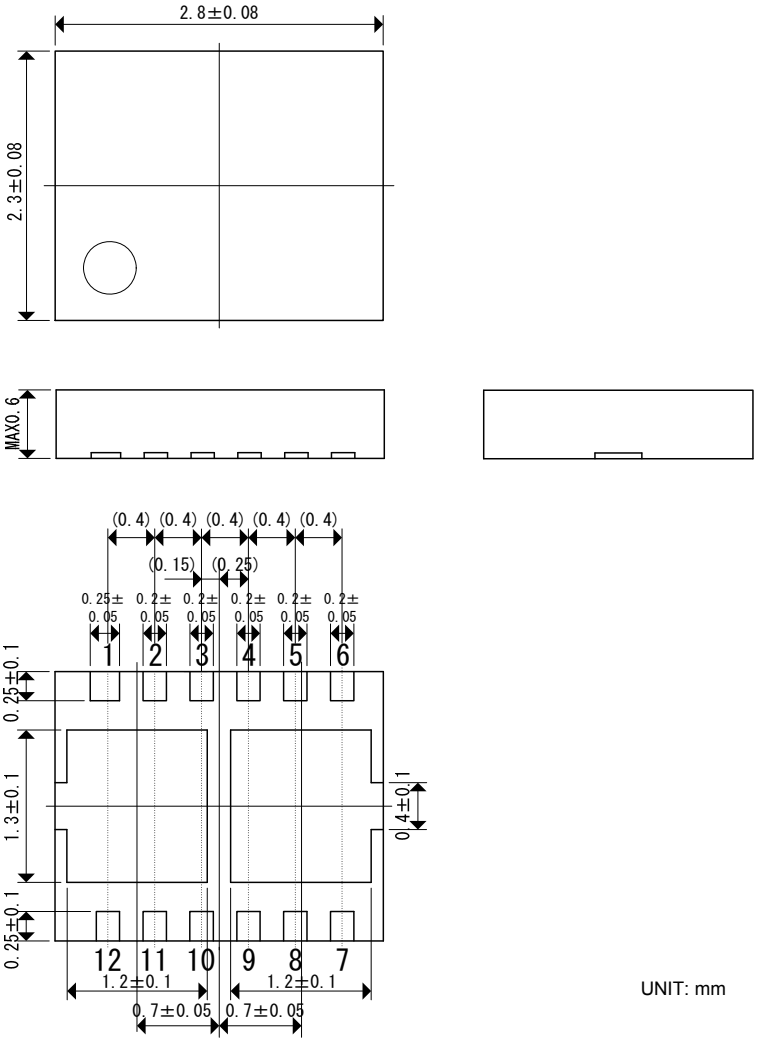
$V_{OUT1}$ : 3.0V & $V_{OUT2}$ : 2.85V

$V_{IN1}$=4.0V, $C_{IN1}$=$C_{L1}$=$C_{L2}$=1 μF(ceramic)



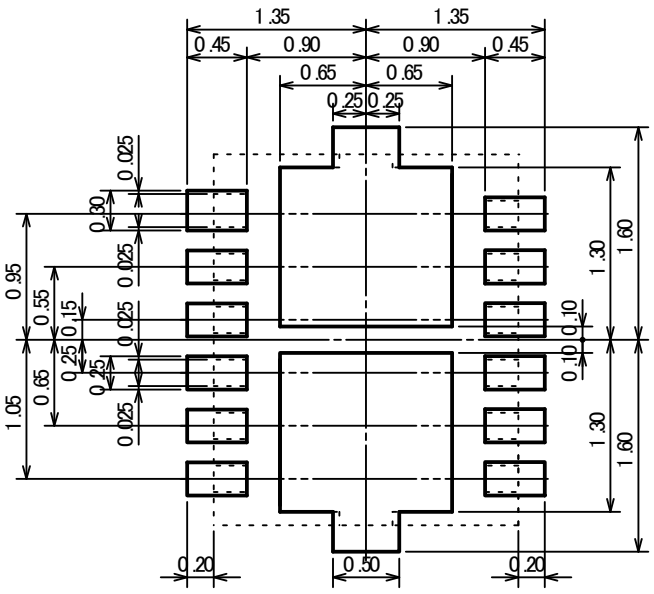
# ■PACKAGING INFORMATION

●USP-12B01

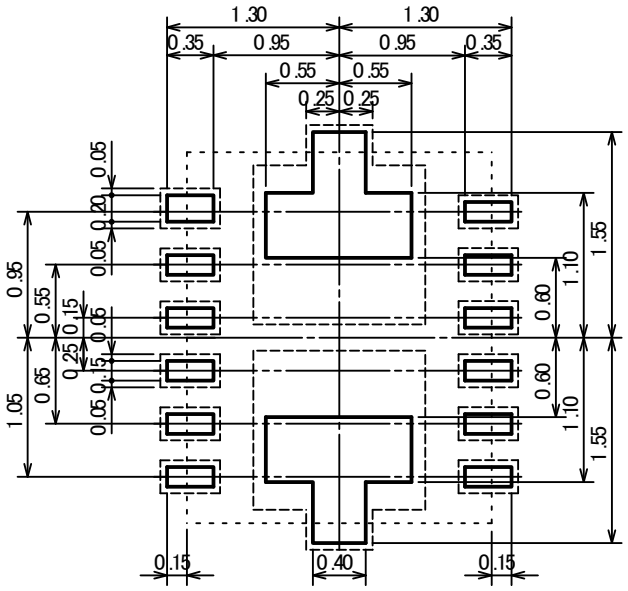



UNIT: mm

●USP-12B01 Reference Pattern Layout




●USP-12B01 Reference Metal Mask Design



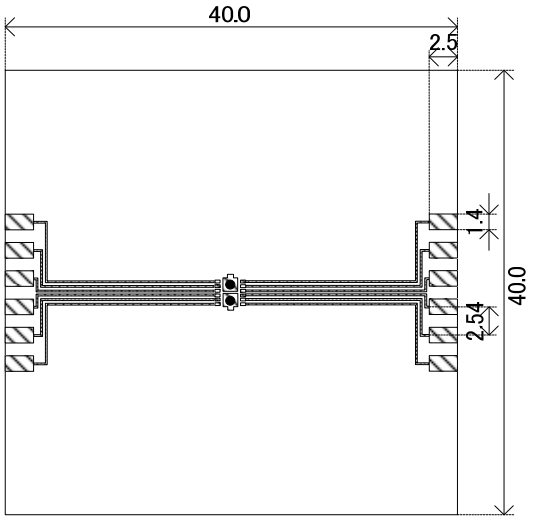
## ■PACKAGING INFORMATION (Continued)

● USP-12B01 Power Dissipation

Power dissipation data for the USP-12B01 is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as one of reference data taken in the described condition.

1. Measurement Condition (Reference data)

Condition: Mount on a board
Ambient: Natural convection
Soldering: Lead (Pb) free
Board: Dimensions 40 x 40 mm (1600 $mm^2$ in one side)
1st Layer: Land and a wiring pattern
2nd Layer: Connecting to approximate 50% of the 1st heat sink
3rd Layer: Connecting to approximate 50% of the 2nd heat sink
4th Layer: Noting
Material: Glass Epoxy (FR-4)
Thickness: 1.6 mm
Through-hole: 2 x 0.8 Diameter (each TAB needs one through-hole)

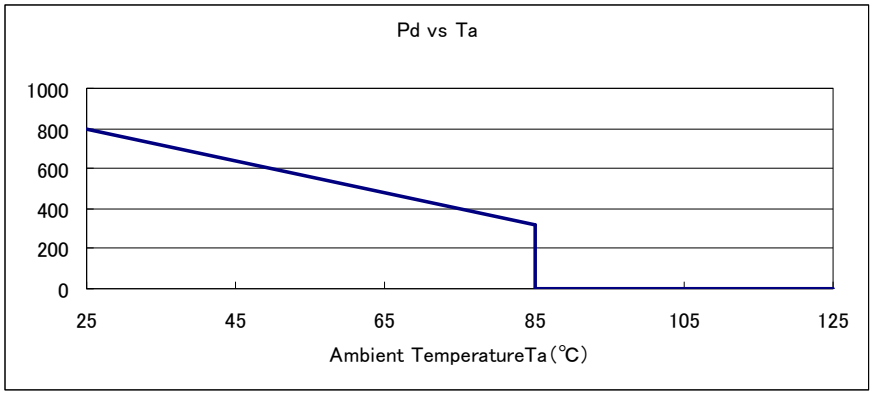



Evaluation Board (Unit: mm)

2. Power Dissipation vs. Ambient temperature

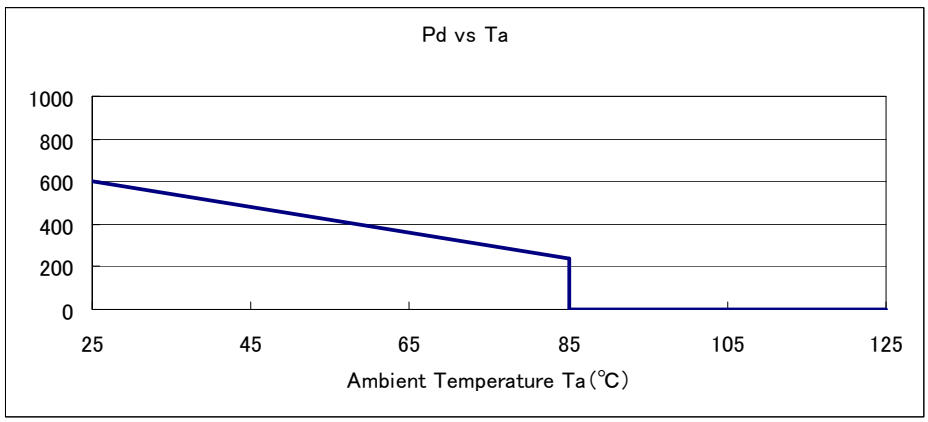
●Only 1ch heating, Board Mount (Tj max = 125℃)

| Ambient Temperature(℃) | Power Dissipation Pd(mW) | Thermal Resistance (℃/W) |
|---|---|---|
| 25 | 800 | 125.00 |
| 85 | 320 | |



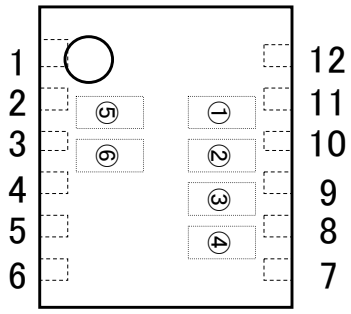

●Both 2ch heating same time, Board Mount (Tj max = 125℃)

| Ambient Temperature(℃) | Power Dissipation Pd(mW) | Thermal Resistance (℃/W) |
|---|---|---|
| 25 | 600 | 166.67 |
| 85 | 240 | |



# ■MARKING RULE

●USP-12B01




USP-12B01

① represents product series

| MARK | PRODUCT SERIES |
|---|---|
| 1 | XCM520 Series |

②③ represents combination of IC

| MARK | | PRODUCT SERIES |
|---|---|---|
| ② | ③ | |
| A | A | XC6401FF**＋XC9235A**D |

④ represents combination of voltage for each IC.

| MARK | PRODUCT SERIES |
|---|---|
| 1 | XCM520**01** |

⑤,⑥ represents production lot number
01～09、0A～0Z、11･･･9Z、
A1～A9、AA･･･Z9、ZA～ZZ repeated
(G, I, J, O, Q, W excluded)
* No character inversion used.

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