XC9711 Series

ETR05094-002

60V 1A Synchronous Step-Down DC/DC Converters

■GENERAL DESCRIPTION

The XC9711 series is 60V bootstrap synchronous step-down DC/DC converter with built-in Nch-Nch driver FETs.

The XC9711 series has operating voltage range of 4.5V~60.0V, the output voltage can be set from 2.5V to 18.0V. It can support 1.0A as an output current with high-efficiency and stable voltage.

The switching frequency is 800kHz, and the operation mode can be selected between PWM control and PWM/PFM control with the MODE pin. When PWM control is operated, the frequency is constant regardless of the load, so noise countermeasures are easy. PWM/PFM control can achieve high efficiency from light loads to heavy loads.

The same part number can be used for multiple power supply lines because the set value of the output voltage can be changed using an external resistor.

It is possible to externally adjust the soft-start time longer than the internal soft-start using an external resistor and capacitor connected to EN/SS pin.

In addition, the power good function monitors the state of the output voltage. The soft start external adjustment function and power good function make it easy to configure the power supply sequence.

Built-in protection functions include current limit, over voltage protection, thermal shutdown and Lx short protection for safety operation.

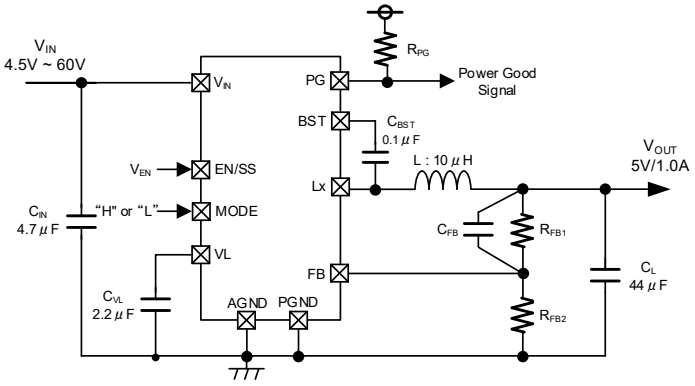
■APPLICATIONS

- 24V Battery Systems
- Industrial Automation
- Industrial Sensors
- Security Systems
- Home Appliances / Power Tools
- High-Voltage LDO Replacement
- General-Purpose Power-circuit / Point-of-load

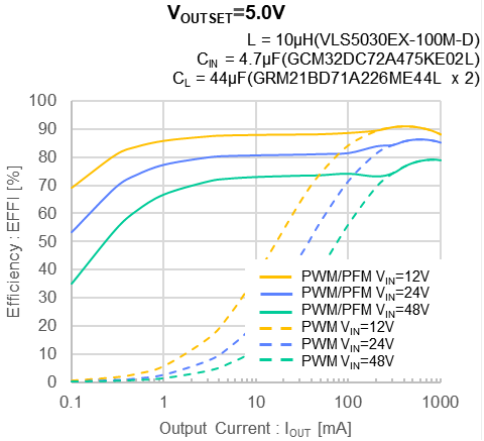
■FEATURES

Input Voltage Range	:	4.5V ~ 60.0V (Absolute Max 61.5V)
Output Voltage Range	:	2.5V ~ 18.0V
FB Voltage	:	0.75V±1.5%
Maximum Output Current	:	1.0A
Oscillation Frequency	:	800kHz
Control Methods	:	PWM control (MODE="H") PWM/PFM control (MODE="L")
Protection Functions	:	Current Limit (Foldback) Output Over Voltage Protection Thermal Shutdown Lx short protection
Functions	:	Power Good, UVLO Soft-start (external adjustment)
Output Capacitor	:	Ceramic Capacitor
Operating ambient temperature	:	-40 ~ 125℃/ Tjmax=150℃
PKG	:	DFN3030-12A (3.0 x 3.0 x 0.75mm) HSOP-8N (6.2 x 5.2 x 1.7mm)
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

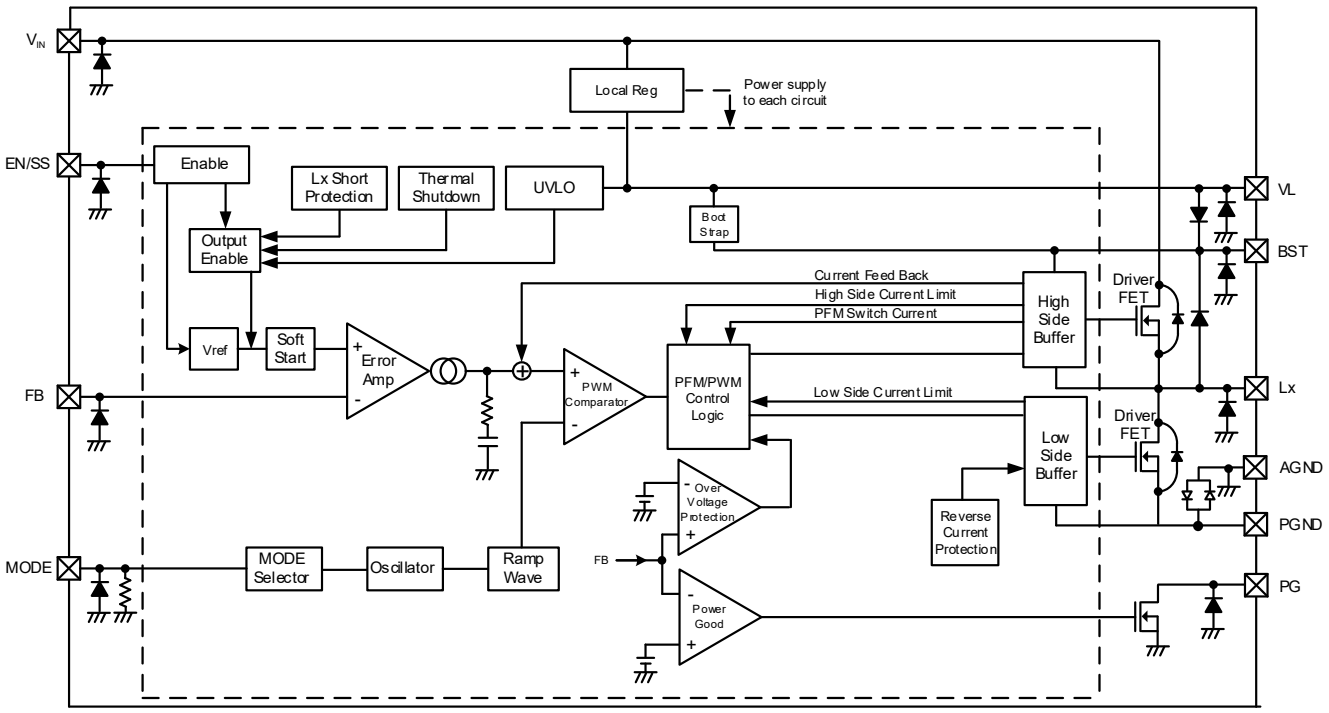
■TYPICAL APPLICATION CIRCUIT



■TYPICAL PERFORMANCE CHARACTERISTICS



■BLOCK DIAGRAM



* Diodes inside the circuit are ESD protection diodes and parasitic diode.

■PRODUCT CLASSIFICATION

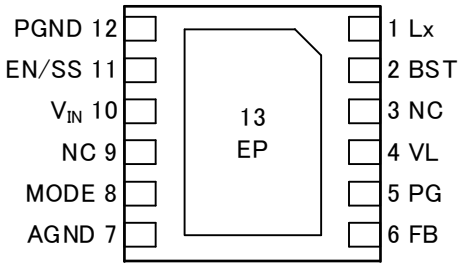
●Ordering Information

XC9711①②③④⑤⑥-⑦(*1)

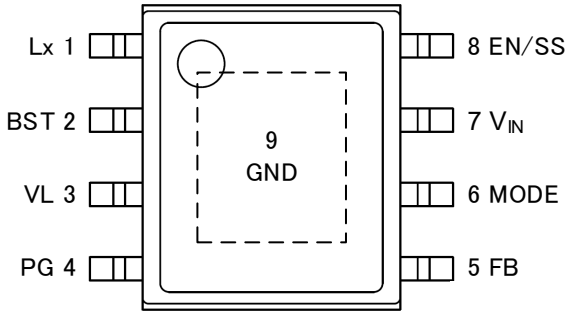
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	-
②③	FB Voltage	75	0.75V
④	Oscillation Frequency	8	800kHz
⑤⑥-⑦(*1)	Packages (Order Unit)	6R-G	DFN3030-12A (3,000pcs/Reel)
		RR-G	HSOP-8N (1,000pcs/Reel)

(*1) The “-G” suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

■PIN CONFIGURATION



DFN3030-12A (Bottom View)



HSOP-8N (TOP View)

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
DFN3030-12A	HSOP-8N		
1	1	Lx	Switching
2	2	BST	Bootstrap
4	3	VL	Local Regulator
5	4	PG	Power Good Output
6	5	FB	Output Voltage Sense
7	-	AGND	Analog Ground
8	6	MODE	Operation Mode Select
10	7	V_{IN}	Power Input
11	8	EN/SS	Enable / Soft-Start
12	-	PGND	Power Ground
-	9	GND	Ground
3,9	-	NC	No Connection
13	-	EP	Exposed thermal pad. The exposed pad must be connected to GND (Pin7,12)

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	H	Active
	L	Stand-by
	OPEN	Stand-by
MODE	H	PWM
	L	PWM/PFM Auto
	OPEN	PWM/PFM Auto

PIN NAME	CONDITION		SIGNAL
PG	EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
		$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
		Over Voltage Protection	H (High impedance)
		Thermal Shutdown	L (Low impedance)
		UVLO ($V_{IN} < V_{UVLOD}$)	Undefined State
	EN/SS = L	Stand-by	L (Low impedance)

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage		V_{IN}	-0.3 ~ 61.5	V
EN/SS Pin Voltage		$V_{EN/SS}$	-0.3 ~ 61.5	V
FB Pin Voltage		V_{FB}	-0.3 ~ 6.5	V
VL Pin Voltage		V_{VL}	-0.3 ~ V_{IN} + 0.3 or 6.5	V
VL Pin Current		I_{VL}	10	mA
MODE Pin Voltage		V_{MODE}	-0.3 ~ 6.5	V
PG Pin Voltage		V_{PG}	-0.3 ~ 6.5	V
PG Pin Current		I_{PG}	2	mA
BST Pin Voltage		V_{BST}	-0.3 ~ V_{LX} + 6.5	V
Lx Pin Voltage		V_{LX}	-0.3 ~ V_{IN} + 0.3 or 61.5 (*1)	V
Power Dissipation	DFN3030-12A	Pd	2050 (JESD51-7 Board) (*2)	mW
	HSOP-8N		3125 (JESD51-7 Board) (*2)	
Junction Temperature		Tj	-40 ~ 150	℃
Storage Temperature		Tstg	-55 ~ 150	℃

All voltages are described based on the GND (AGND, PGND) pin.

(*1) The maximum value should be either V_{IN}+0.3V or 61.5V in the lowest.

(*2) The power dissipation figure shown above is based upon PCB mounted and it is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNITS
Output Voltage Setting Range		V_{OUTSET}	2.5	-	18.0	V
Input Voltage		V_{IN}	4.5	-	60.0	V
Output Current		I_{OUT}	0	-	1000	mA
EN/SS Voltage		$V_{EN/SS}$	0.0	-	60.0	V
VL Pin Current		I_{VL}	Do not connect to external load.			-
MODE Pin Voltage		V_{MODE}	0.0	-	6.0	V
PG Pull-up Voltage		V_{PG}	0.0	-	6.0	V
PG Pull-up Resistor		R_{PG}	5	200	-	kΩ
Operating Ambient Temperature		Topr	-40	-	125	℃
Input Capacitor (Effective Value)		C_{IN}	1.2	-	1000 (*2)	μF
Output Capacitor (Effective Value)	2.5V≦V_{OUTSET}≦6.0V	C_L	16.0	-	1000 (*3)	μF
	6.0V＜V_{OUTSET}≦12.0V		12.0	-	1000 (*3)	
	12.0V＜V_{OUTSET}≦18.0V		10.0	-	1000 (*3)	
Local Regulator Capacitor (Effective Value)		C_{VL}	1.55	2.20	2.85	μF
Bootstrap Capacitor (Effective Value)		C_{BST}	0.075	0.100	0.125	μF

GND(AGND, PGND) are standard voltage for all the voltage.

(*1) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*2) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase, and the IC may malfunction.

(*3) If using a large-capacity capacitor as the output capacitance, output stability may decrease and ripple voltage may increase. Even within the recommended capacitance range, output stability may be reduced depending on the type of capacitor such as ESR etc. used, so please verify this fully on the actual equipment before using.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS	CIRCUIT
Operating Input Voltage Range	V_{IN}			4.5	-	60.0	V	-
Setting Output Voltage Range	V_{OUTSET}			2.5	-	18.0	V	-
FB Voltage	V_{FB}	V_{FB}=0.768V→0.732V V_{FB} when Lx pin oscillates, V_{MODE}=5V		0.739	0.750	0.761	V	①
Local Regulator Output Voltage	V_{VL}	I_{VL}=0.1mA, V_{FB}=0.785V		4.75	5.00	5.25	V	②
UVLO Detect Voltage	V_{UVLOD}	V_{IN}=4.5V→3.3V, $V_{EN/SS}$=5V, V_{FB}=0.675V V_{IN} voltage when Lx pin holds “L” level		3.515	3.700	-	V	①
UVLO Release Voltage	V_{UVLOR}	V_{IN}=3.3V→4.5V, $V_{EN/SS}$=5V, V_{FB}=0.675V V_{IN} voltage when Lx pin changes from "L" to "H" level		-	4.000	4.200	V	①
Quiescent Current PFM	I_{q_PFM}	V_{FB}=0.785V, V_{LX}=0V, V_{MODE} =0V		-	9	22	μA	①
Quiescent Current PWM	I_{q_PWM}	V_{FB}=0.785V, V_{LX}=0V, V_{MODE}=5V		-	370	490	μA	①
Stand-by Current	I_{STB}	$V_{EN/SS}$=V_{FB}=V_{LX}=0V, V_{MODE}=0V		-	0.8	2.0	μA	①
Oscillation Frequency	f_{OSC}	V_{FB}=0.675V		720	800	880	kHz	①
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.675V		85	90	-	%	①
Minimum Duty Cycle	D_{MIN}	V_{FB}=0.785V		-	-	0	%	①
Lx ”H” SW On Resistance	R_{LXH}	I_{LX}=100mA		-	420	620	mΩ	-
Lx ”L” SW On Resistance	R_{LXL}	I_{LX}=100mA		-	250	-	mΩ	-
PFM Switch Current	I_{PFM}	Connection to external components, I_{OUT}=1mA, V_{IN}=12V		-	400	-	mA	③
High side Current Limit	I_{LIMH}	V_{FB}=0.75V		1400(*1)	2000(*1)	2600(*1)	mA	-
Internal Soft-Start Time	t_{ss1}	V_{FB}=0.675V		1.0	2.0	4.5	ms	①
External Soft-Start Time	t_{ss2}	V_{FB}=0.675V, R_{ss}=390kΩ, C_{ss}=0.47μF		-	8.8	-	ms	④
FB Voltage Temperature Characteristics	ΔV_{FB} / (ΔT_{opr}* V_{FB})	-40≦T_{opr}≦125℃		-	±100	-	ppm/℃	①
Over Voltage Protection	V_{OVP}	V_{FB}=0.75V→0.9V, Lx pin voltage holding “L” level		0.796	0.829	0.862	V	-
PG Detect Voltage	V_{PGDET}	V_{FB}=0.75V→0.6V, R_{PG} =200kΩ pull-up to 5V V_{FB} when PG pin voltage changes from “H” level to “L” level.		0.630	0.667	0.704	V	⑤
PG Output Voltage	V_{PG}	V_{FB}=0.675V, I_{PG}=1mA		-	0.05	0.3	V	⑥
EN “H” Voltage	V_{ENH}	V_{FB}=0.675V, $V_{EN/SS}$ which Lx pin oscillates	Ta=25℃	2.5	-	60.0	V	①
			Ta=-40~125℃	2.5(*2)	-	60.0		
EN “L” Voltage	V_{ENL}	V_{FB}=0.675V, $V_{EN/SS}$ which Lx pin voltage holding “L” level	Ta=25℃	GND	-	0.4	V	①
			Ta=-40~125℃	GND	-	0.4(*2)		
EN “H” Current	I_{ENH}	V_{IN}=$V_{EN/SS}$=60V		-	0.06	0.15	μA	⑦
EN “L” Current	I_{ENL}	V_{IN}=60V, $V_{EN/SS}$=0V		-	0.0	0.1	μA	⑦
Thermal Shutdown Temperature	T_{TSD}	Junction Temperature		-	160	-	℃	-
Hysteresis Width	T_{HYS}	Junction Temperature		-	25	-	℃	-
MODE “H” Voltage	V_{MODEH}	Operation MODE “PWM/PFM Auto” to “PWM”	Ta=25℃	1.2	-	6.0	V	③
			Ta=-40~125℃	1.5(*2)	-	6.0		
MODE “L” Voltage	V_{MODEL}	Operation MODE “PWM” to “PWM/PFM Auto”	Ta=25℃	GND	-	0.45	V	③
			Ta=-40~125℃	GND	-	0.3(*2)		
MODE “H” Current	I_{MODEH}	V_{MODE}=5V		-	2.5	5.5	μA	⑦
MODE “L” Current	I_{MODEL}	V_{MODE}=0V		-	0.0	0.1	μA	⑦
FB “H” Current	I_{FBH}	V_{IN}=$V_{EN/SS}$=60V, V_{FB}=1V		-	0.0	0.1	μA	⑦
FB “L” Current	I_{FBL}	V_{IN}=$V_{EN/SS}$=60V, V_{FB}=0V		-	0.0	0.1	μA	⑦
Lx "H" Leakage Current	I_{LXH}	V_{IN}=60V, V_{LX}=0V, $V_{EN/SS}$=V_{FB}=0V		-	0.0	0.1	μA	⑧
Lx "L" Leakage Current	I_{LXL}	V_{IN}=60V, V_{LX}=60V, $V_{EN/SS}$=V_{FB}=0V		-	0.0	0.1	μA	⑧

Test Condition: Unless otherwise stated, V_{IN}=24V, $V_{EN/SS}$=24V

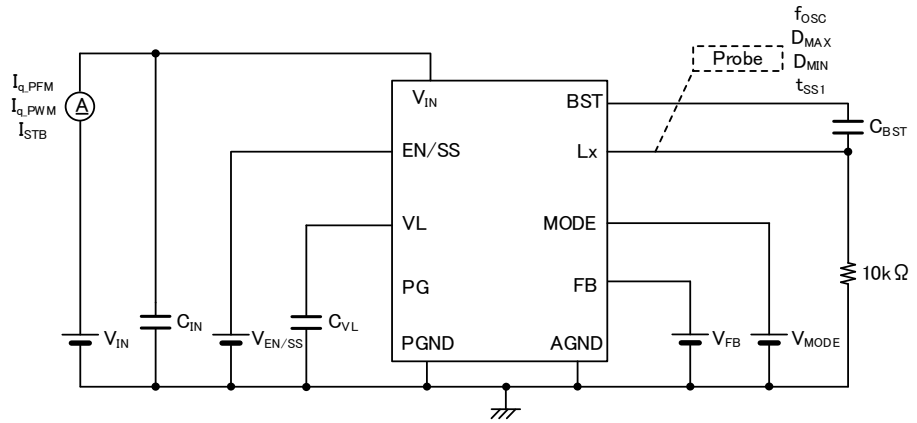
Connected to external components : L=10μH, R_{FB1}=680kΩ, R_{FB2}=120kΩ, C_{FB}=15pF, C_L=44μF, C_{IN}=4.7μF, C_{VL}=2.2μF, C_{BST}=0.1μF

*1: Current limit denotes the level of detection at top of coil current.

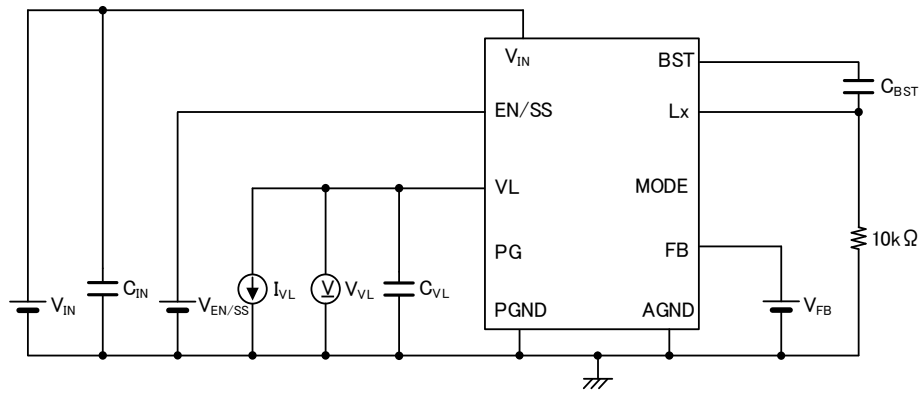
*2: Design value

■TEST CIRCUITS

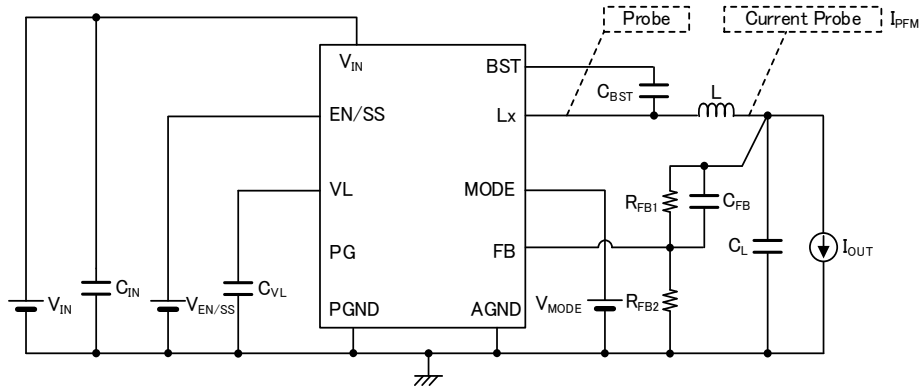
TEST CIRCUIT①



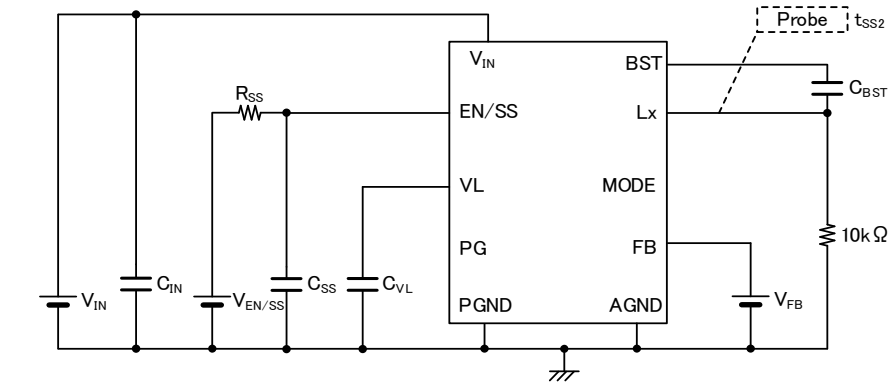
TEST CIRCUIT②



TEST CIRCUIT③

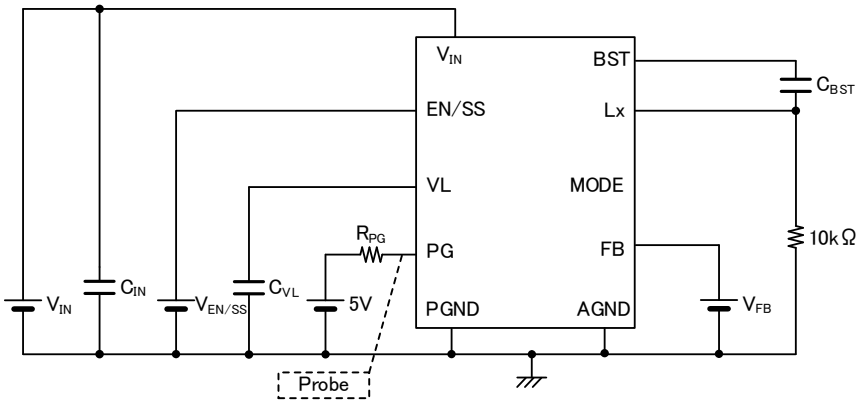


TEST CIRCUIT④

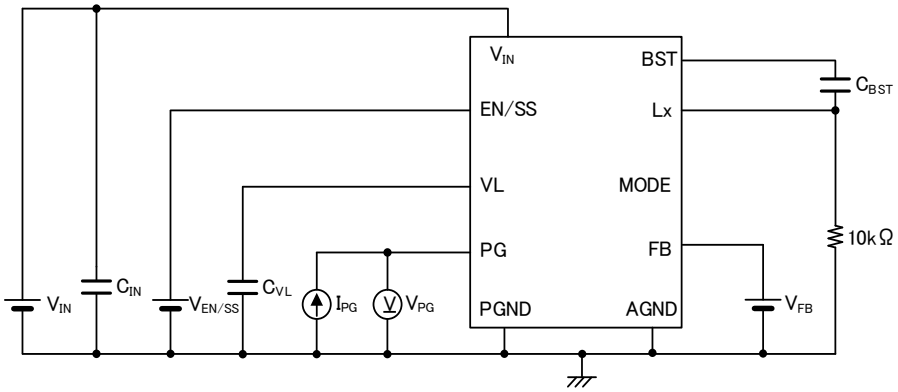


■TEST CIRCUITS

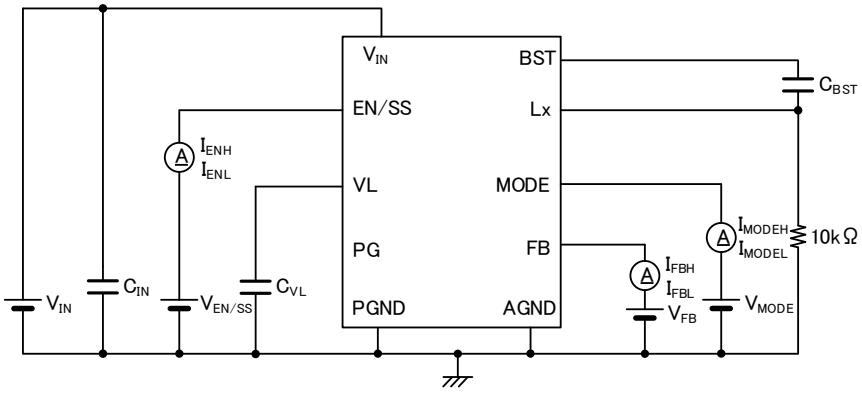
TEST CIRCUIT⑤



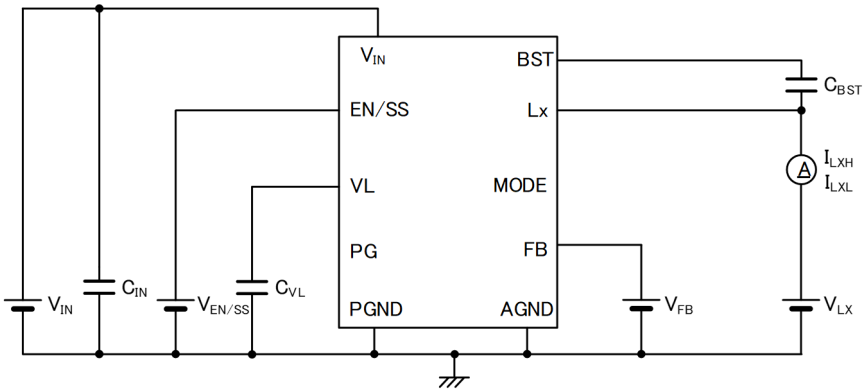
TEST CIRCUIT⑥



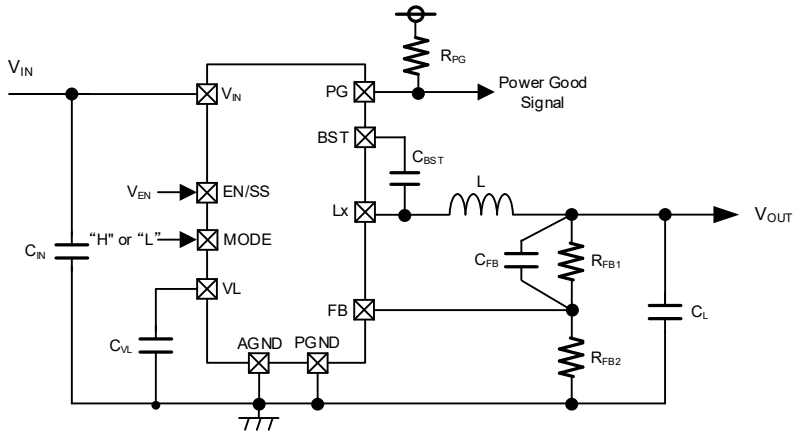
TEST CIRCUIT⑦



TEST CIRCUIT⑧



■TYPICAL APPLICATION CIRCUIT / PARTS SELECTION GUIDE



	CONDITIONS	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE(L×W×T)
L	V_{OUTSET}≦6.0V	TDK	VLS5030EX-100M-D	10μH	5.3×5.0×3.0mm
	6.0V＜V_{OUTSET}≦12.0V	TDK	VLS5045EX-220M-H	22μH	5.3×5.0×4.5mm
	12.0V＜V_{OUTSET}	TDK	VLS6045EX-330M-H	33μH	6.3×6.0×4.5mm

	CONDITIONS	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE(L×W×T)
C_{IN}	-	TDK	C3225X7S2A475K200AB	4.7μF/100V	3.2×2.5×2.2mm
		Murata	GCM32DC72A475KE02L	4.7μF/100V	3.2×2.5×2.2mm
C_L	V_{OUTSET}≦6.0V	TDK	C2012X6S1C226M125AC	22μF/16V x 2	2.0×1.25×1.45mm
		Murata	GRM21BD71A226ME44L	22μF/10V x 2	2.0×1.25×1.45mm
	6.0V＜V_{OUTSET}≦12.0V	TDK	C2012X7S1E106KT	10μF/25V x 3	2.0×1.25×1.50mm
	12.0V＜V_{OUTSET}	TDK	C3216X7R1H106K160AC	10μF/50V x 2	3.2×1.6×1.90mm
C_{BST}	-	TDK	C1005X7R1E104K050BB	0.1μF	1.0×0.5×0.55mm
		Murata	GCM155R71H104KE02D	0.1μF	1.0×0.5×0.55mm
C_{VL}	-	TDK	C1608X7S1E225K080AB	2.2μF	1.6×0.8×1.0mm
		Murata	GRM188C71E225KE11D	2.2μF	1.6×0.8×1.0mm

(*1) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*2) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase, and the IC may malfunction.

■TYPICAL APPLICATION CIRCUIT / PARTS SELECTION GUIDE

<Output voltage setting Value>

The output voltage can be set by adding an external dividing resistor.

The output voltage (V_{OUTSET}) is determined by the equation below based on the values of R_{FB1} and R_{FB2}.

$$V_{OUTSET} = V_{FB} \times (R_{FB1}+R_{FB2}) / R_{FB2}$$

However, $R_{FB2} \leqq 250k\Omega$ and $R_{FB1}+R_{FB2} \leqq 2M\Omega$

If the IC does not operate normally due to external noise, etc., noise resistance performance can be improved by using a combination of R_{FB1} and R_{FB2} smaller than the above conditional expression.

< C_{FB} setting>

The value of the speed-up capacitor C_{FB} is optimized by adjusting with the following equation.

The optimum value of f_{zfb} does not change regardless of the capacitance value of the output capacitor.

$$C_{\mathrm{FB}} = \frac{1}{2\pi \times f_{\mathrm{zfb}} \times R_{\mathrm{FB1}}}$$

$$f_{\mathrm{zfb}} = 16\mathrm{kHz}$$

【Calculation Example】

When the output voltage is set to 5.0V, R_{FB1}=680kΩ, R_{FB2}=120kΩ, V_{OUTSET}=0.75V×(680kΩ+120kΩ) / 120kΩ = 5.0V.

Since the target is f_{zfb}=16kHz, C_{FB}= 1/(2× π ×16kHz×680kΩ) =14.6pF from the above equation, which is 15pF for the E24 series.

PWM/PFM control (MODE='L' or 'OPEN'): Typical Examples

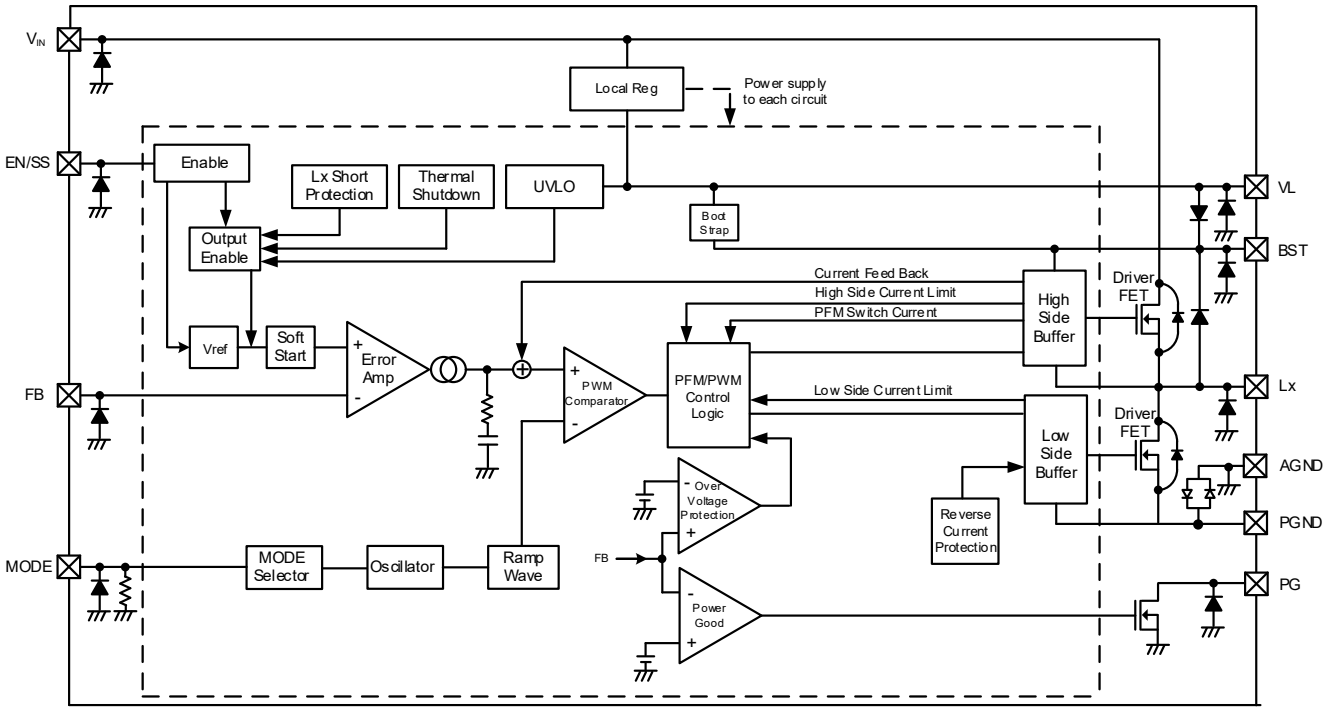
V_{OUTSET}	R_{FB1}	R_{FB2}	C_{FB}	f_{zfb}
2.5V	560kΩ	240kΩ	18pF	15.8kHz
3.3V	680kΩ	200kΩ	15pF	15.6kHz
5.0V	680kΩ	120kΩ	15pF	15.6kHz
6.0V	910kΩ	130kΩ	12pF	14.6kHz
12.0V	750kΩ	51kΩ	12pF	17.7kHz
15.0V	820kΩ	43kΩ	12pF	16.2kHz
18.0V	620kΩ	27kΩ	15pF	17.1kHz

PWM control(MODE="H") : Typical Examples

V_{OUTSET}	R_{FB1}	R_{FB2}	C_{FB}	f_{zfb}
2.5V	56kΩ	24kΩ	180pF	15.8kHz
3.3V	68kΩ	20kΩ	150pF	15.6kHz
5.0V	68kΩ	12kΩ	150pF	15.6kHz
6.0V	91kΩ	13kΩ	120pF	14.6kHz
12.0V	75kΩ	5.1kΩ	120pF	17.7kHz
15.0V	82kΩ	4.3kΩ	120pF	16.2kHz
18.0V	62kΩ	2.7kΩ	150pF	17.1kHz

■OPERATIONAL EXPLANATION

The control method of this IC is a current mode control method compatible with low ESR ceramic capacitors.



<Internal power supply (Local Reg)>

This IC has a built-in regulator as an internal power supply for supplying voltage to the internal circuit.

The output of the regulator is output to the VL pin, and the VL pin voltage becomes V_{VL} (TYP. 5.0V). However, when the V_{IN} pin voltage becomes lower than V_{VL}, the regulator output voltage will drop.

Even when EN/SS='L', internal regulator operates, and voltage is supplied to the internal circuit.

In addition to the internal circuit, the regulator supplies voltage to the BST pin via a backflow prevention switch.

The internal regulator has an output short circuit protection function.

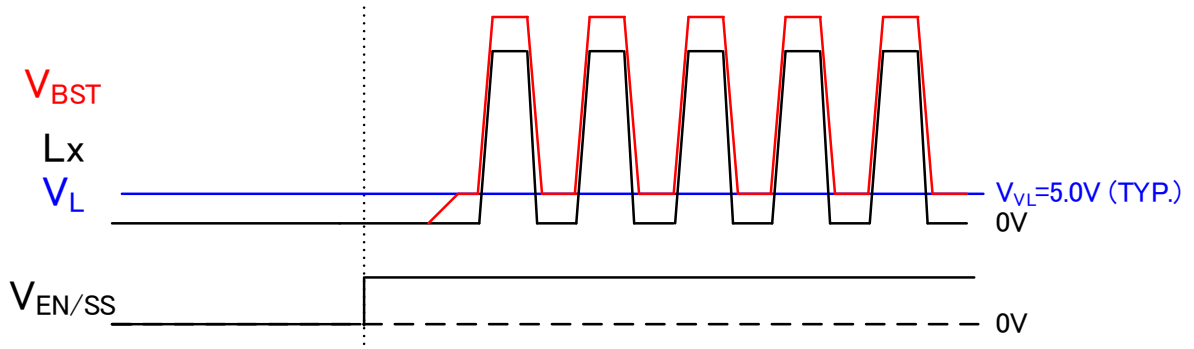
When the VL pin is shorted during regulator operation, or when the regulator is started with the VL pin already shorted, the output current of the regulator is controlled to prevent overcurrent from flowing. If the output short is released during regulator operation, it will automatically recover.

Note that using the VL pin voltage for purposes other than this IC is prohibited.

<Bootstrap>

This IC uses an Nch FET as the High side driver FET and has a built-in bootstrap circuit for generating its gate voltage.

During the on-time of the low-side driver FET (Lx≒0V), an external capacitor C_{BST} is charged by the internal power supply. The BST pin voltage is used as the power supply voltage for the high-side buffer circuit. Due to the external capacitor C_{BST}, the BST pin voltage is maintained at "Lx + V_{VL} (TYP. 5.0V)" even during the off-time of the low-side driver FET. It is possible to supply the gate voltage necessary for driving the high-side driver FET.



■OPERATIONAL EXPLANATION

<Normal operation>

The error amplifier compares the internal reference voltage Vref divided by resistance with FB pin voltage. And the control signal obtained by adding phase compensation to the output of the error amplifier is input to the PWM comparator to determine the switching ON time during PWM control.

The PWM comparator compares the above control signal with the ramp wave, and outputs a switching pulse with a controlled duty width from the Lx pin. The output voltage is stabilized by performing these controls continuously.

The current sense circuit monitors the current of the driver FET for each switching operation and modulates the output signal of the error amplifier as a multiple feedback signal (current feedback circuit). This enables stable feedback control even using a low ESR capacitor such as a ceramic capacitor.

PWM control (MODE="H")

During MODE='H', the system operates in forced PWM mode.

Due to operating at a constant frequency f_{OSC} (TYP. 800kHz) regardless of the current output, it becomes easy to filter switching noise.

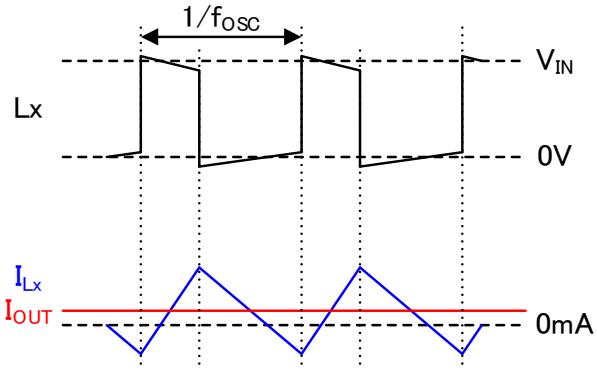
In addition, when the FB pin voltage keeps higher than V_{FB}, the switching stops (turns off the High-side/Low-side driver), and it stops until the FB pin voltage drops.

PWM/PFM automatic switching control (MODE='L' or 'OPEN')

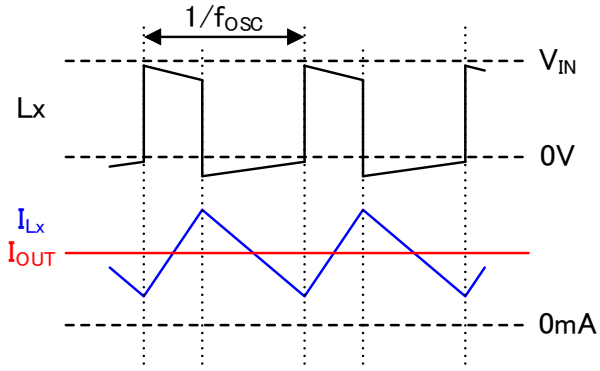
When MODE='L' or OPEN, it operates in PWM/PFM automatic switching mode.

PWM/PFM automatic switching control reduces the switching frequency at light load by turning on the High side driver FET until the coil current reaches the PFM current I_{PFM} (TYP. 400mA).

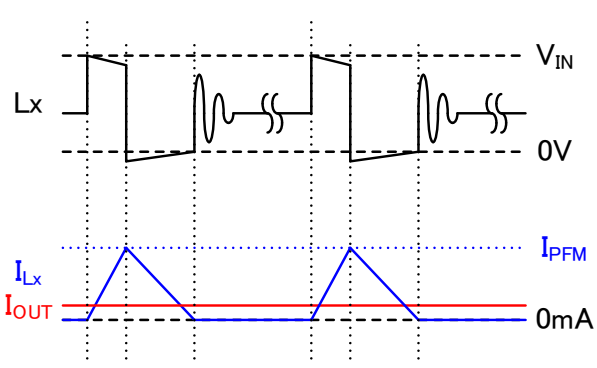
This operation reduces loss of light loads and achieves high efficiency from light loads to heavy loads. When the output current increases, the switching frequency increases in proportion to the output current. When the switching frequency reaches f_{OSC}, PFM control is switched to PWM control, and the switching frequency is fixed.



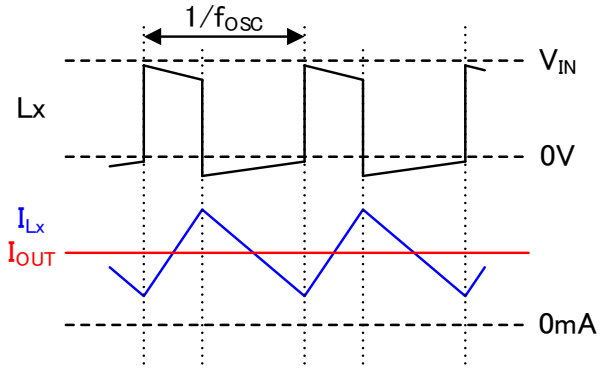
PWM control : operation example of light loads



PWM control : operation example of heavy loads



PWM/PFM control : operation example of light loads



PWM/PFM control : operation example of heavy loads

■OPERATIONAL EXPLANATION

<EN Function / Start Mode・Soft-start Function>

The state of the IC can be switched by applying voltage to the EN/SS pin.

PIN NAME	SIGNAL	STATUS
EN/SS	H	Active
	L	Stand-by
	OPEN	Stand-by

EN/SS='L' or 'OPEN': Stand-by mode

When the EN/SS pin voltage is "L" or "OPEN", the IC enters the stand-by mode, and the current consumption is reduced to the stand-by current I_{STB} (TYP. 0.8μA). In the stand-by mode, no signal is output to the Lx pin and the output voltage does not rise. In addition, various protection functions stop operating.

The internal regulator operates even in the stand-by state, but the output voltage of the regulator is lower than the active state voltage V_{VL} (TYP. 5.0V).

EN/SS="H": Active mode

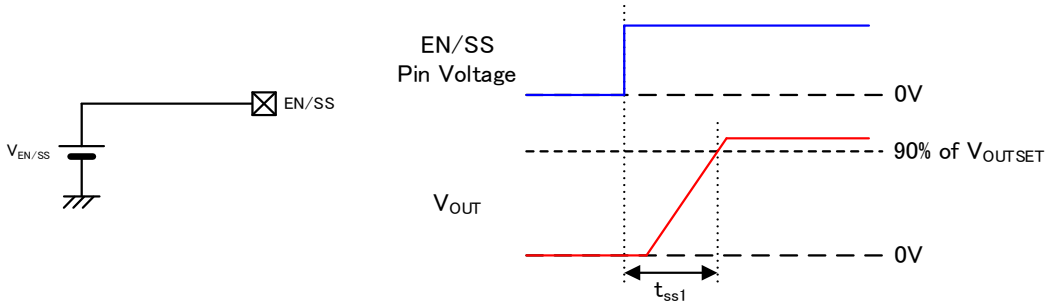
When the EN/SS pin voltage is "H", the IC becomes active. When the IC becomes active, it enters start-up mode and increases the output voltage to the set output voltage.

In start-up mode, a soft-start function is provided to gently raise the output voltage to suppress inrush current at start-up. The soft-start time can be adjusted by externally mounting a capacitor and resistor on the EN/SS pin.

During the start-up mode, the device operates in the same way as in normal operation, except that the reference voltage increases linearly.

(a) Internal soft-start time (no external RC)

When the EN/SS pin voltage rises steeply, the output voltage rises with an internally set soft-start time of t_{ss1} (TYP. 2.0ms) and shifts to normal mode.



■OPERATIONAL EXPLANATION

(b) Soft-start time external adjustment (with external RC)

The soft-start time can be adjusted by externally mounting a capacitor and resistor on the EN/SS pin.

The externally set soft-start time (t_{SS2}) is determined by the following formula, depending on the EN/SS pin voltage ($V_{EN/SS}$), R_{SS}, and C_{SS} values.

$$t_{ss2} = C_{ss} \times R_{ss} \times \ln \frac{V_{EN/SS}}{V_{EN/SS} - (1.25 \times 0.9)}$$

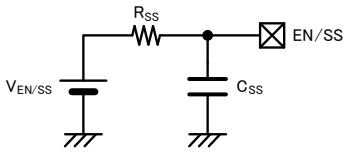
For example, When the soft-start time at C_{SS} = 0.47μF, R_{SS} = 390kΩ, $V_{EN/SS}$ = 24V, the result is as follows.

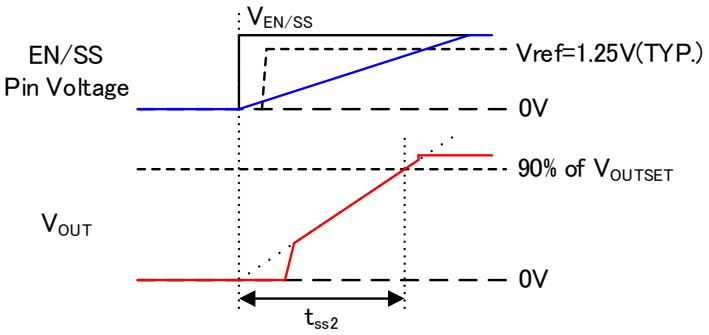
$$t_{ss2} = 0.47 \times 10^{-6} \times 390 \times 10^{3} \times \ln \frac{24}{24 - (1.25 \times 0.9)} = 8.8\text{ms}$$

However, it cannot start faster than the internally setting soft-start time t_{ss1}.

Please avoid using an extremely high resistance value for the external resistor as R_{SS} and use an R_{SS} that satisfies the following equation.

$$R_{ss} \leq \frac{V_{EN/SS} - 2.5\text{V}}{12\mu\text{A}}$$





* Definition of soft-start time: Time from $V_{EN/SS}$ start-up until output voltage reaches 90% of set output voltage.

■OPERATIONAL EXPLANATION

<Current Limit>

The current limit circuit of this IC detects the current flowing through the driver FET connected to Lx and equivalently monitors the coil current. The current limit function operates when overcurrent is detected. The current limiting function includes a high side current limiting function and a low side current limiting function. The current limit state continues until the overcurrent state is released, and the output voltage automatically recovers when the overcurrent state is released.

A current fold-back circuit is used for the current limit function.

In a current fold-back circuit, the output voltage drops, and the current limit is held down when the FB voltage drops. This operation results in a narrowing of the output current when the output voltage drops.

High side Current Limit

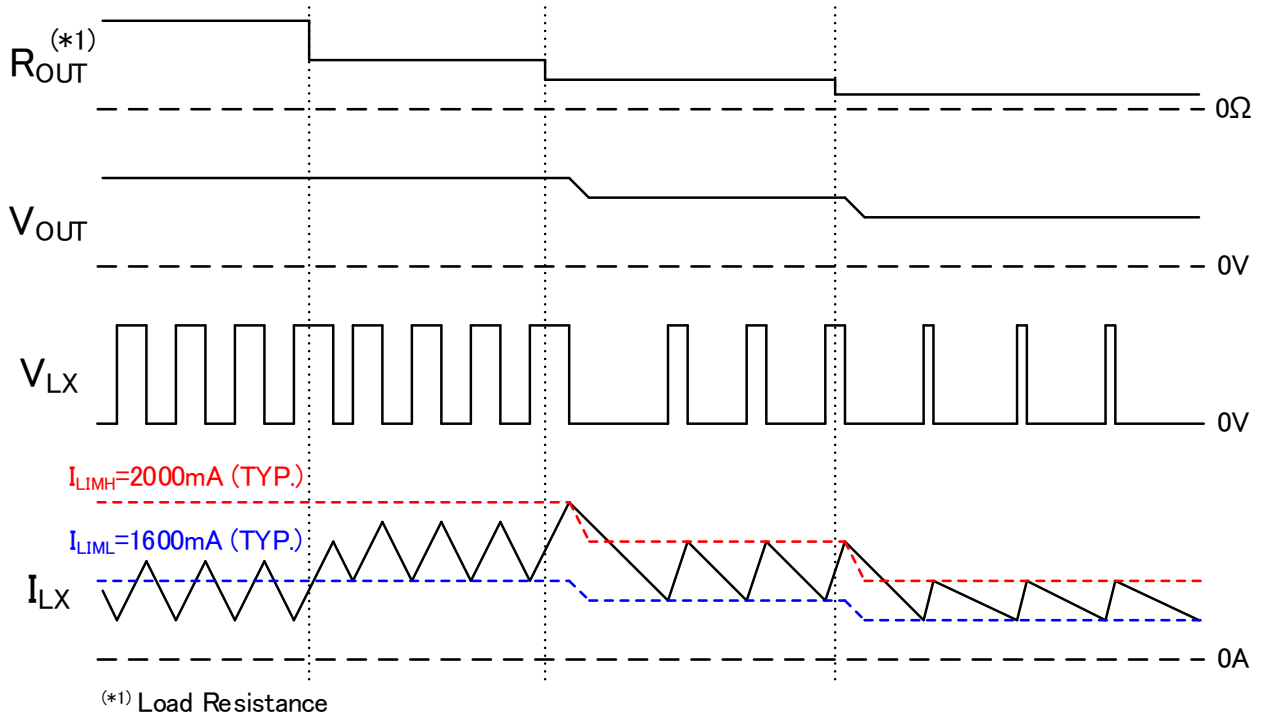
The High side current limit function detects when the coil current exceeds the High side current limit value I_{LIMH} (TYP. 2000mA) and turns off the High side driver FET. In other words, it controls the coil current peak so that it does not exceed I_{LIMH}. However, if the input voltage is high, the coil current peak value may exceed I_{LIMH} due to the operation delay of the internal circuit.

Low side Current Limit

The Low side current limit function turns on the Low side driver FET until the coil current becomes less than the Low side current limit value I_{LIML} (TYP. 1600mA). In other words, it controls the bottom of the coil current below I_{LIML}.

The current limit function also operates during start-up mode.

During start-up mode, the output voltage is lower than the set output voltage, the current limit value is reduced, which speeds up overcurrent detection. If an output capacitance with a higher effective capacitance value than the recommended component is used, the start-up will take place while the current limit function is operating, and the start-up time may be much longer than the soft-start time.



■OPERATIONAL EXPLANATION

<Thermal Shutdown>

The junction temperature is monitored to protect the IC from thermal destruction.

When the junction temperature reaches the thermal shutdown detection temperature T_{TSD} (TYP. 160°C), the thermal shutdown activated, the High side driver FET and Low side driver FET are turned off. When the junction temperature drops to the thermal shutdown release temperature T_{TSD}-T_{HYS} (TYP. 135°C) by stopping the current supply, the output voltage is turned on by the start-up mode, and then normal operation starts.

The internal regulator operates even during thermal shutdown, and the output voltage V_{VL} (TYP. 5.0V) is output to the VL pin.

<UVLO>

This function monitors the internal power supply of the IC and prevents false pulse output from the Lx pin due to unstable operation when the internal power supply is low. As the IC's internal power supply drops as the V_{IN} pin voltage drops, the UVLO function operates when the V_{IN} pin voltage drops.

When the V_{IN} pin voltage falls below V_{UVLOD} (TYP. 3.7V), the UVLO function operates, and forcibly turns off the driver FETs. When the V_{IN} pin voltage rises above V_{UVLOR} (TYP. 4.0V), the UVLO function is released, and the output voltage rises according to the start-up mode.

During UVLO operation, the internal regulator is still operating, and its output voltage approximately matches the V_{IN} pin voltage. However, if the V_{IN} pin voltage is so low that the regulator or the reference voltage Vref cannot operate, the regulator output voltage will be less than the V_{IN} pin voltage.

<Over Voltage Protection>

An output overvoltage protection function is built in to suppress output voltage overshoots after completion of start-up or transient response. When the FB pin voltage rises above V_{FB} x 1.105 (TYP.), the output overvoltage protection function operates and forcibly turns off the High side driver FET.

In forced PWM control (MODE="H"), the Low side driver FET is turned on immediately after the output overvoltage protection function operates and remains in this state until the next cycle.

In PWM/PFM automatic switching control (MODE="L" or OPEN), the driver FET is turned off by the output overvoltage protection function. When the output voltage drops to the set value due to the current output, switching operation resumes.

<Lx Short Protection>

If the Lx pin is shortened to GND during normal operation, the Lx short protection function will operate.

The Lx short protection function turns off the driver FET to prevent IC breakdown due to overcurrent.

After the Lx short protection function operates, the output voltage rises in start-up mode, but if the Lx pin remains short to GND, the output voltage does not rise because the Lx short protection function is operated again during start-up mode.

If the IC starts up with the Lx pin short to GND, the Lx short protection function also operates, and the output voltage does not rise.

■OPERATIONAL EXPLANATION

<Power Good>

Functions for monitoring the status of outputs and ICs.

CONDITIONS		SIGNAL
EN/SS=H	$V_{FB} > V_{PGDET}$	H (High impedance)
	$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
	Over Voltage Protection	H (High impedance)
	Thermal Shutdown	L (Low impedance)
	UVLO ($V_{IN} < V_{UVLOD}$)	Undefined State
EN/SS=L or OPEN	Stand-by	L (Low impedance)

Since the PG pin is an Nch open-drain output, connect a pull-up resistor (approx. 200kΩ) to the PG pin.
When the power good function is not used, connect the PG pin to GND or leave it open.

A delay time of 600μs (TYP.) is provided from the moment, the FB pin voltage drops below V_{PGDET} to PG="L". If the FB pin voltage returns to a voltage higher than V_{PGDET} during the delay time, PG remains “H”. This prevents PG="L" due to output undershoots during transient response. In addition, there is no intentional delay for PG="L" due to the operation of the protection function or transition to the stand-by state.

<MODE switching function>

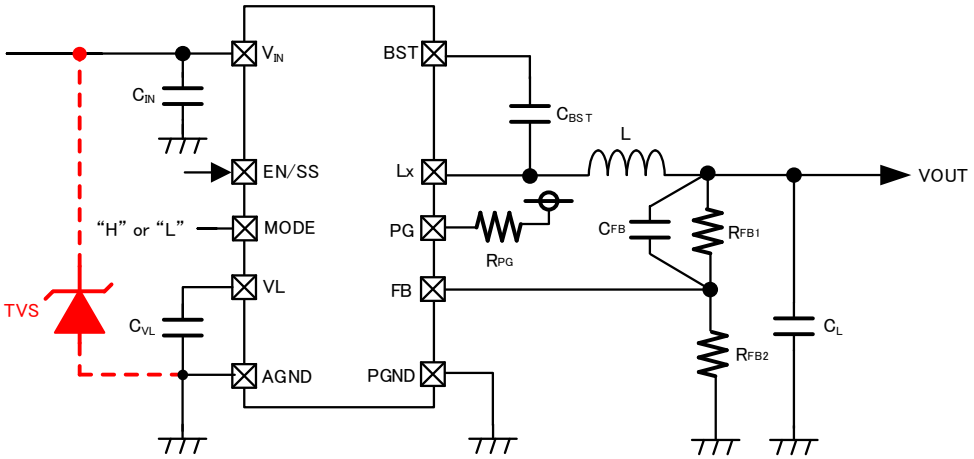
The operation mode can be selected from PWM and PWM/PFM control according to the voltage applied to the MODE pin.
In addition, operation mode is allowed to be switched during normal operation by changing the voltage applied to the MODE pin.

PIN NAME	SIGNAL	STATUS
MODE	H	PWM
	L	PWM/PFM Auto
	OPEN	PWM/PFM Auto

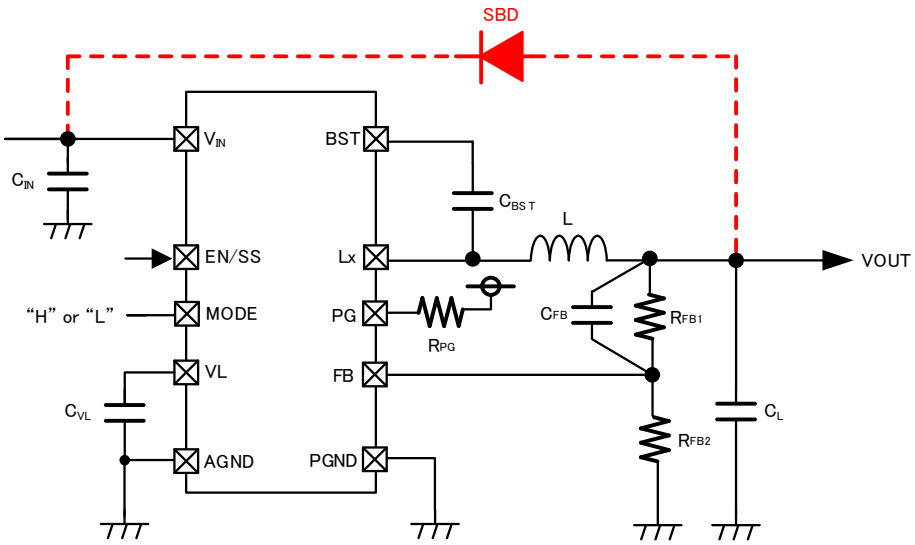
■NOTES ON USE

1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications. Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.

If a voltage exceeding the absolute maximum voltage is applied to this IC due to chattering by mechanical switches or surge voltage from external sources, take measures using protective elements such as TVS and protective circuits.



Under conditions where the input voltage is lower than the output voltage, an overcurrent may flow through the parasitic diode inside the IC and exceed the absolute maximum rating of the Lx pin. If the impedance between V_{IN} and GND is low and current is drawn into the input side, take measures such as adding an SBD between V_{OUT} and V_{IN}.



2) Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the coil inductance, capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

3) The DC/DC converter performance is greatly influenced by not only the ICs' characteristics, but also by those of the external components. Care must be taken when selecting the external components. Especially for capacitors, particular attention should be paid to DC bias characteristics, temperature characteristics, etc. to ensure that they have an effective capacitance equal to or greater than that of the recommended components under actual operating conditions.

■NOTES ON USE

4) Stable operating range

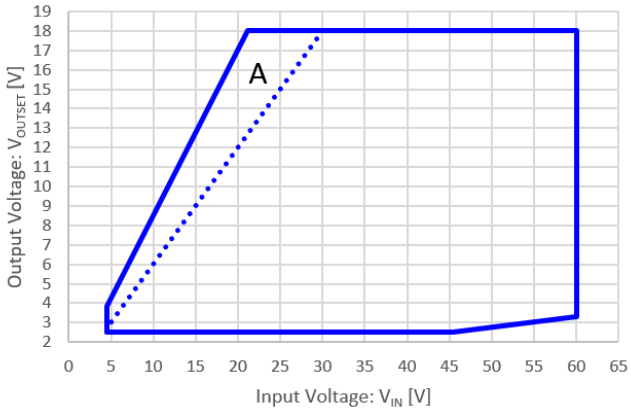
When operating in PWM mode (MODE = 'H'), the oscillation may become unstable under high step-down ratios (when the high-side driver FET's on-time is short). This IC supports stable step-down operation from V_{IN}=60V to V_{OUT}=3.3V (minimum stable on-time: 69ns).

However, at output currents below 100mA where the coil current flows in reverse, stability may decrease and ripple voltage of 2% or less of the output voltage may occur.

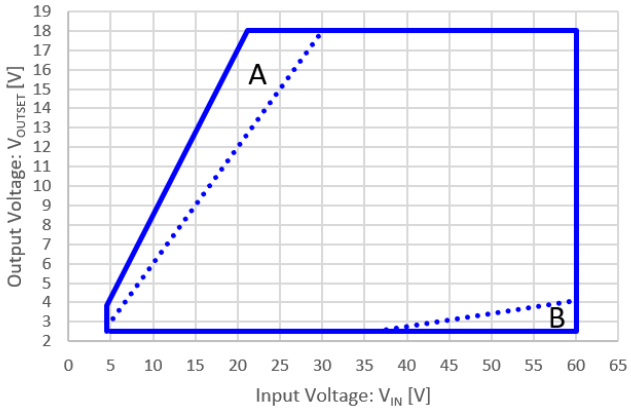
Based on the minimum stable on-time mentioned above, the stable operating range is as follows.

V_{OUTSET}-V_{IN} Stable operating range

PWM Mode(MODE='H')



Automatic PWM/PFM Switching Mode(MODE='L')



However, when operating within the stable range from area A to B, please observe the following precautions

(A) When operated with a duty cycle exceeding 60%, transient response characteristics may significantly deteriorate.

(B) Within this range, even at maximum output current, the device may continue operating in PFM mode without switching to PWM mode.
Furthermore, at output currents above 100mA, output stability may degrade, potentially resulting in large ripple voltages exceeding 10% of the output voltage.

In addition, operating outside the stable range may result in the following behaviors, potentially causing the IC to malfunction.

Operation Outside the Stable Operating Range

(a) Under conditions with a high step-down ratio, abnormal oscillation in the form of a sine wave or pulse skipping may occur.

(b) Under conditions with a low step-down ratio, the device may operate at the maximum duty cycle, resulting in the output voltage dropping below the set output voltage.

5) After soft-start completion, if the input voltage (V_{IN}) is held below the internal power supply voltage (Local Reg): V_{VL} (TYP. 5.0V) and then increased with a slope of 1V/ms or more, the VL pin voltage may overshoot beyond its absolute maximum rating, potentially causing malfunction of the IC.

Under the operating conditions described above, to suppress fluctuations in the VL pin voltage, please use the following components or equivalent parts for C_{VL} instead of the recommended components.

	MANUFACTURER	PRODUCT NUMBER	VALUE	SIZE(L×W×T)
C_{VL}	TDK	C2012X7S1E106KT	10μF/25V	2.0×1.25×1.50mm

6) When using the automatic PWM/PFM switching mode (MODE = 'L' or OPEN), the ripple voltage may increase near the transition point from PFM to PWM operation. Please verify thoroughly using the actual equipment before use.

■NOTES ON USE

7) To ensure proper operation of the IC, supply a stable input voltage to the VIN pin with sufficiently low AC impedance, achieved using a bypass capacitor. If momentary fluctuations in the input voltage occur, consider countermeasures such as increasing the input capacitance.

8) Torex places an importance on improving our products and their reliability. We request that users incorporate fail safe designs and post aging protection treatment when using Torex products in their systems.

9) Instructions for pattern layouts.
Especially noted in the pattern layout are as follows.
Please refer to the reference pattern layout on the next page.

(a) Wire the large current line using thick, short connecting traces.
This makes it possible to reduce the wire impedance, which is expected to reduce noise and improve heat dissipation.
If the wire impedance of the large current line is large, it may cause noise, or the IC cannot operate normally.

(b) Place the input capacitance C_{IN}, output capacitance C_L, inductor L and IC which the large current flows on the same surface. If they are placed on both sides, a large current will flow through Via, which has high impedance, it may cause noise, and the IC may not operate normally.

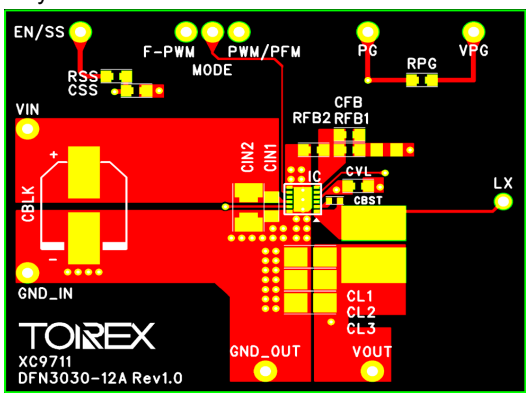
(c) Please mount each external component as close to the IC as possible.
Especially place the input capacitance C_{IN} near the IC and connect it with as low impedance as possible.
If C_{IN} is positioned too far from the IC, it may lead to increased noise or improper operation of the IC.

(d) Since the FB line connected to the FB pin is highly susceptible to noise, please keep the wiring as short as possible. If the FB line is long, the IC may not operate normally due to switching noise and external noise.
In addition, parasitic capacitance may increase due to copper planes or parallel traces located directly beneath the FB line.
This increase in parasitic capacitance can weaken the phase compensation effect provided by CFB, potentially leading to unstable output.
If the IC does not operate properly due to external noise, please consider revising the PCB layout or lowering the FB resistor value.
Note that reducing the FB resistor value may decrease efficiency during PFM operation, so be sure to verify thoroughly with actual equipment.

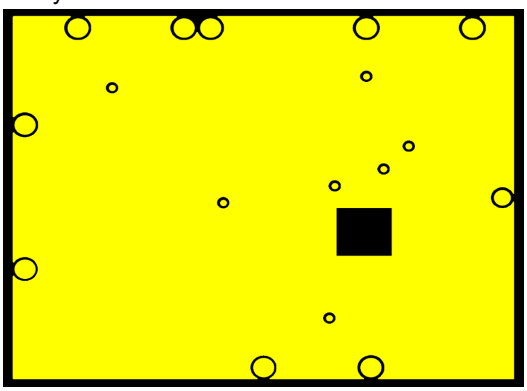
<Pattern layout>

DFN3030-12A

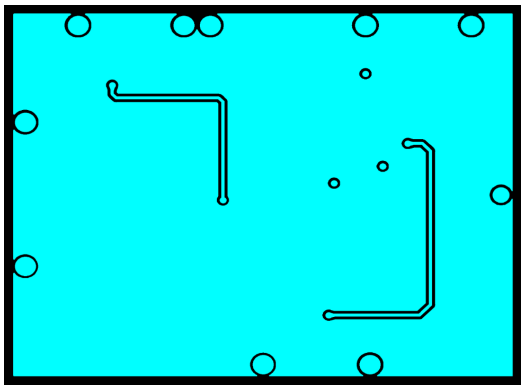
Layer 1



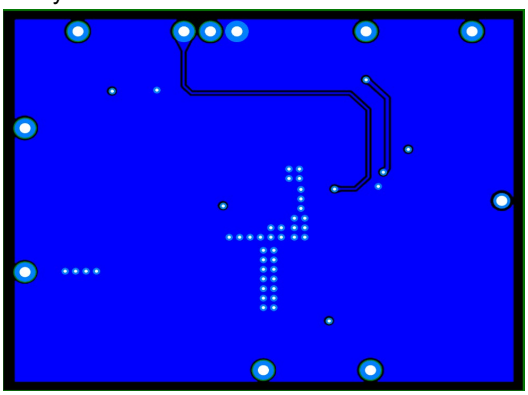
Layer 2



Layer 3

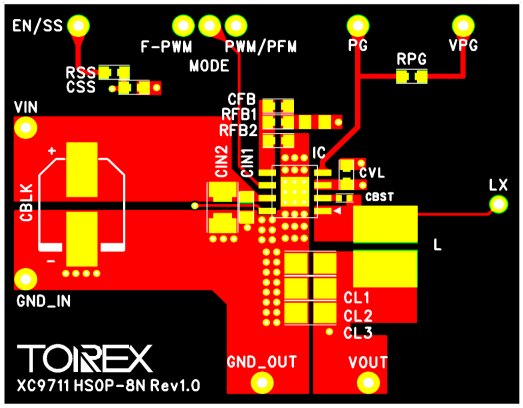


Layer 4

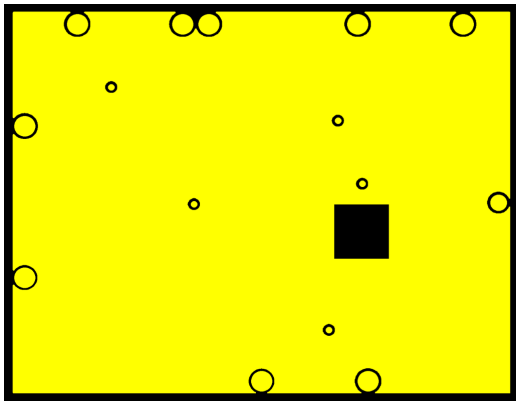


HSOP-8N

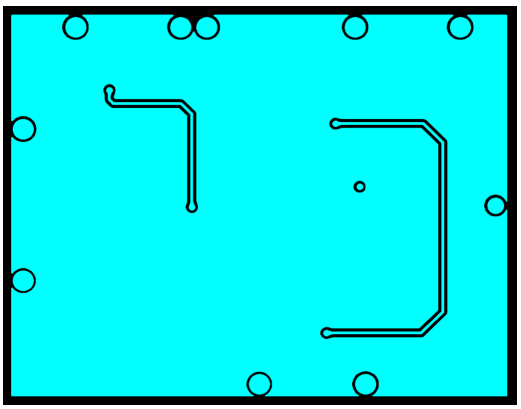
Layer 1



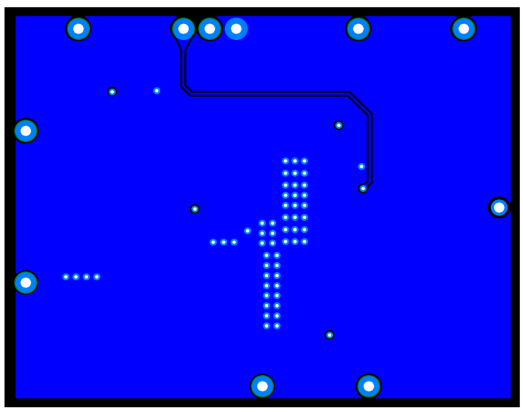
Layer 2



Layer 3



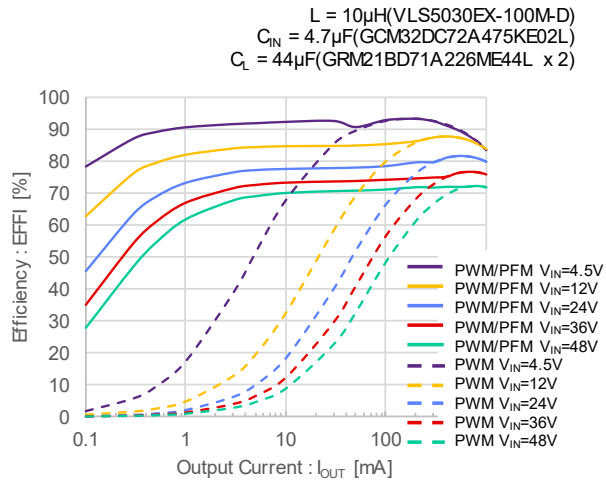
Layer 4



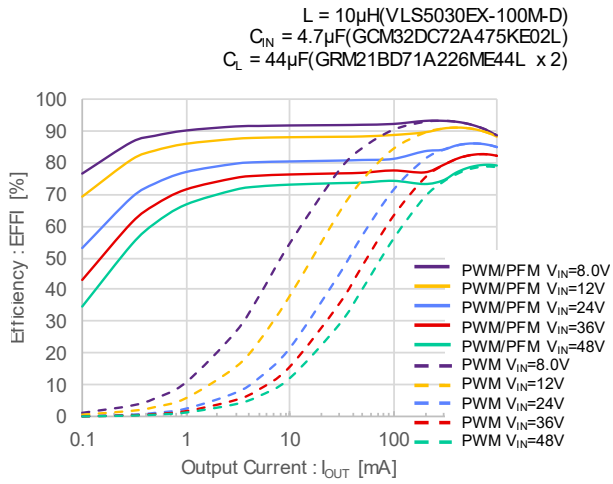
■TYPICAL PERFORMANCE CHARACTERISTICS

(1-1) Efficiency vs. Output Current

V_{OUTSET}=3.3V

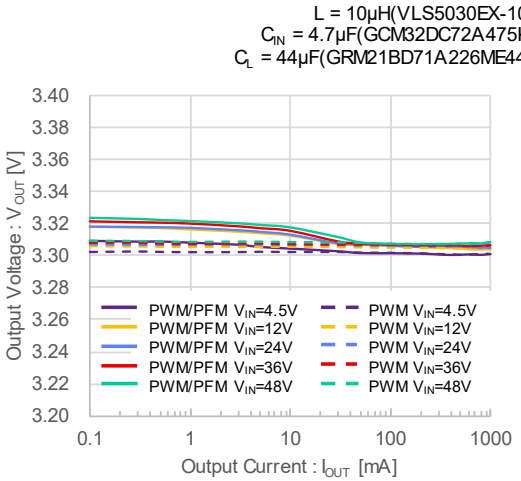


V_{OUTSET}=5.0V

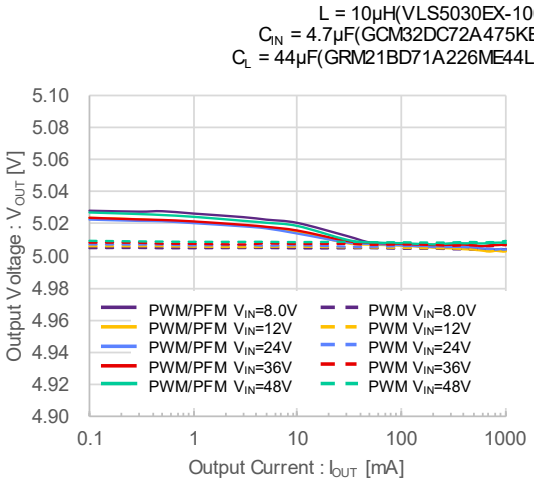


(2-1) Output Voltage vs. Output Current

V_{OUTSET}=3.3V

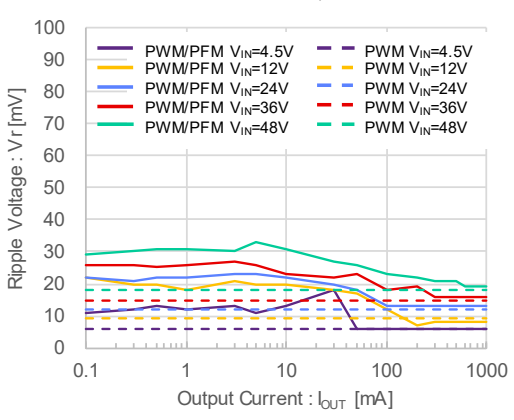


V_{OUTSET}=5.0V

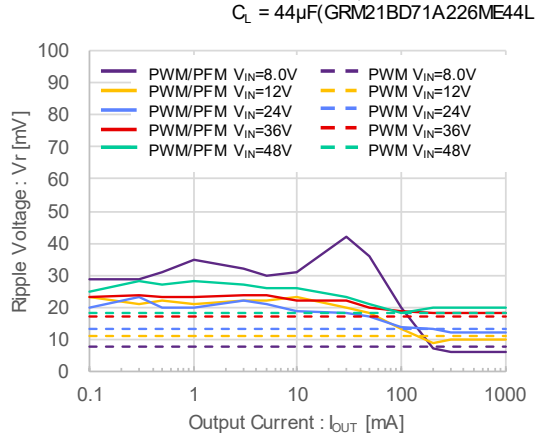


(3-1) Ripple Voltage vs. Output Current

V_{OUTSET}=3.3V



V_{OUTSET}=5.0V

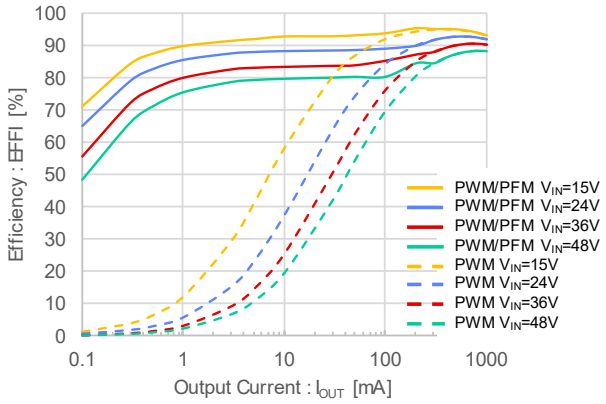


■TYPICAL PERFORMANCE CHARACTERISTICS

(1-2) Efficiency vs. Output Current

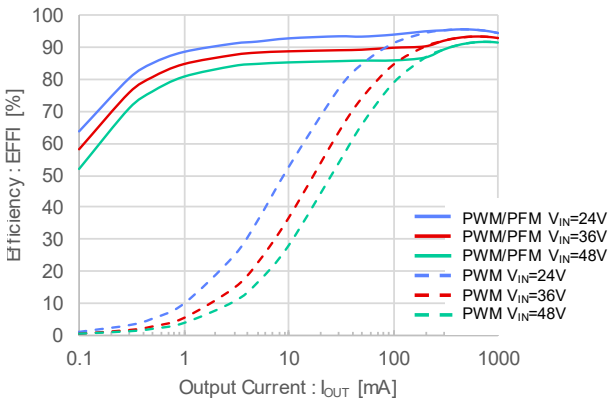
V_{OUTSET}=12V

L = 22μH(VLS5045EX-220M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 30μF(C2012X7S1E106KT x 3)



V_{OUTSET}=18V

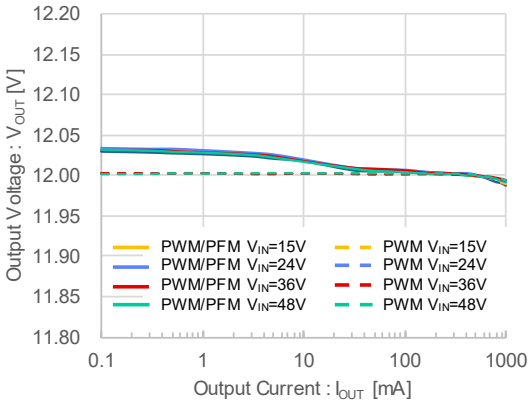
L = 33μH(VLS6045EX-330M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 20μF(C3216X7R1H106K160AC x 2)



(2-2) Output Voltage vs. Output Current

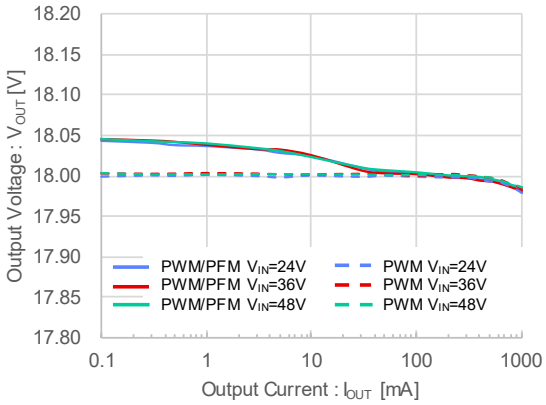
V_{OUTSET}=12V

L = 22μH(VLS5045EX-220M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 30μF(C2012X7S1E106KT x 3)



V_{OUTSET}=18V

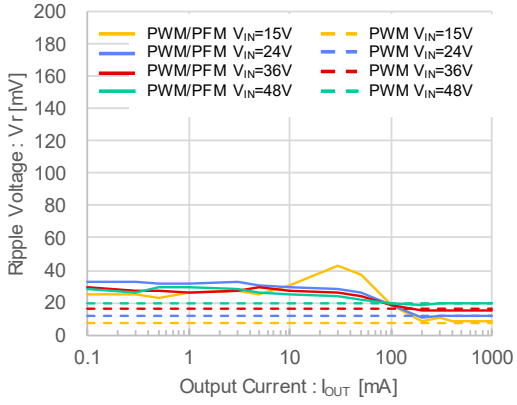
L = 33μH(VLS6045EX-330M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 20μF(C3216X7R1H106K160AC x 2)



(3-2) Ripple Voltage vs. Output Current

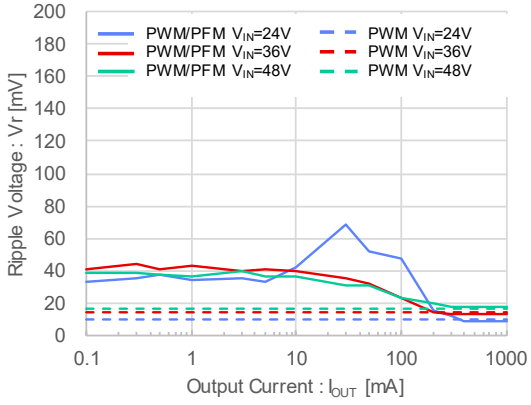
V_{OUTSET}=12V

L = 22μH(VLS5045EX-220M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 30μF(C2012X7S1E106KT x 3)



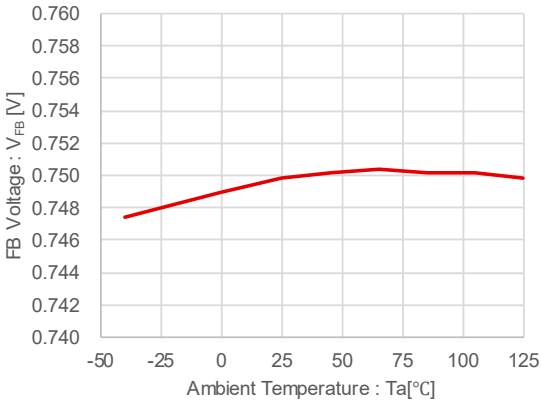
V_{OUTSET}=18V

L = 33μH(VLS6045EX-330M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 20μF(C3216X7R1H106K160AC x 2)

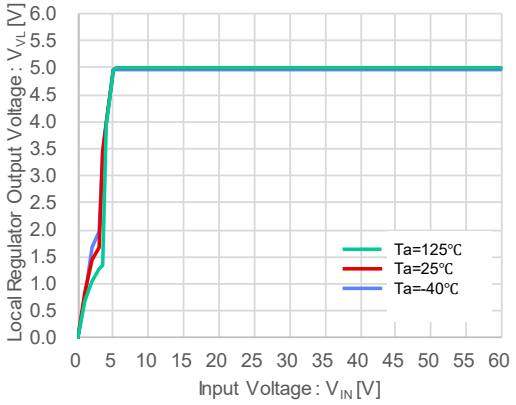


■TYPICAL PERFORMANCE CHARACTERISTICS

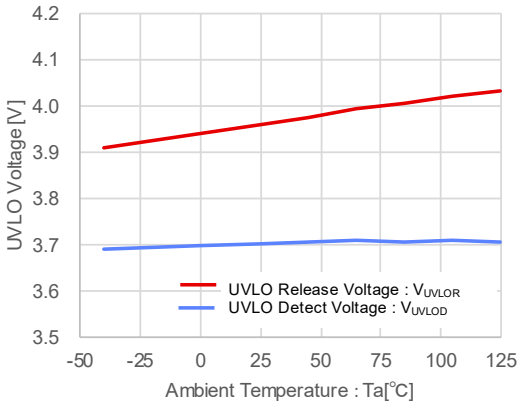
(4) FB Voltage vs. Ambient Temperature



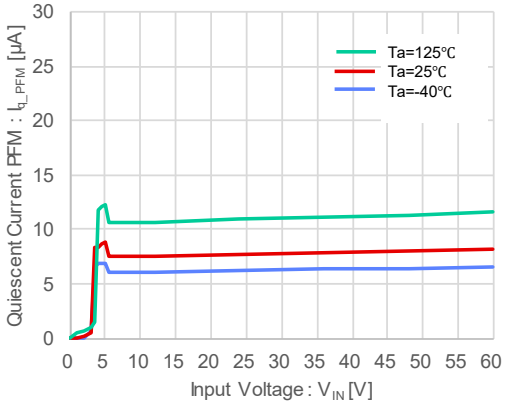
(5) Local Regulator Output Voltage vs. Input Voltage



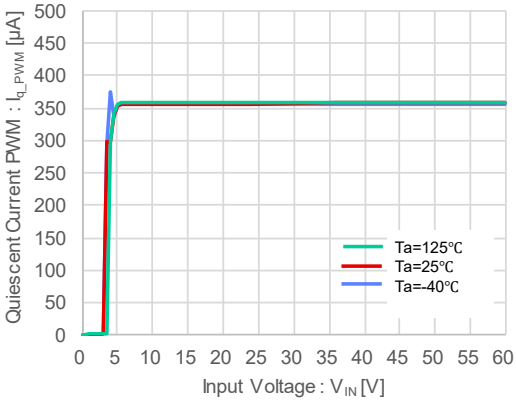
(6) UVLO Voltage vs. Ambient Temperature



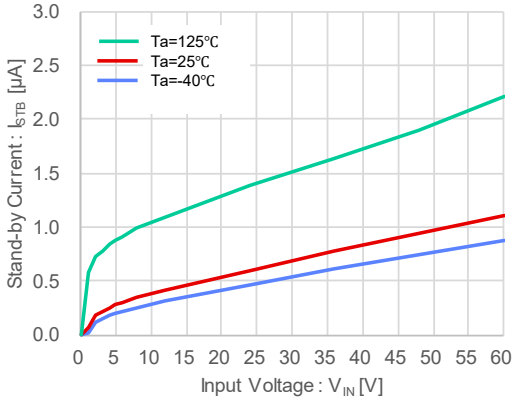
(7) Quiescent Current PFM vs. Input Voltage



(8) Quiescent Current PWM vs. Input Voltage

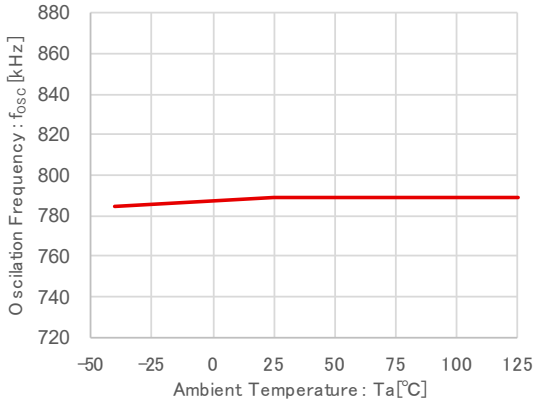


(9) Stand-by Current vs. Input Voltage

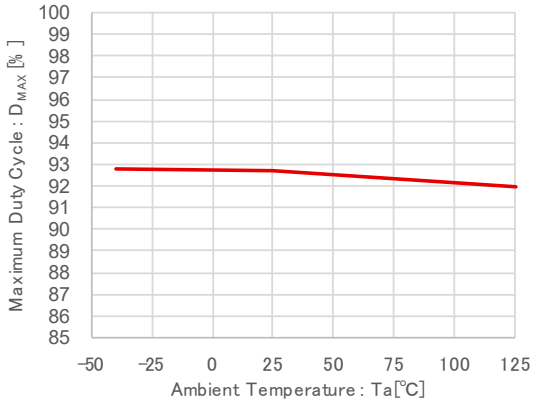


■TYPICAL PERFORMANCE CHARACTERISTICS

(10) Oscillation Frequency vs. Ambient temperture

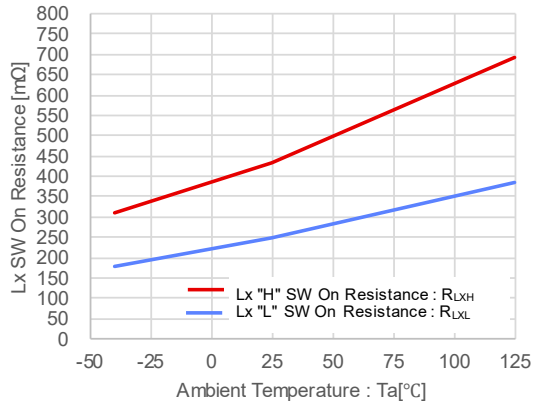


(11) Maximum Duty Cycle vs. Ambient temperture



(12) Lx SW On Resistance vs. Ambient Temperature

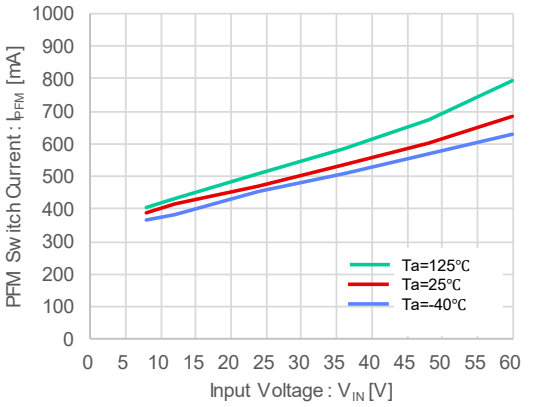
XC9711A7586R-G (DFN3030-12A)



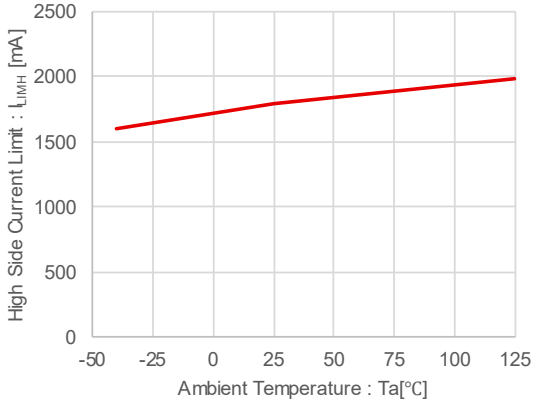
(13) PFM Switch Current vs. Input Voltage

V_{IN}=12.0V, V_{OUTSET}=5.0V, I_{OUT}=1.0mA

L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



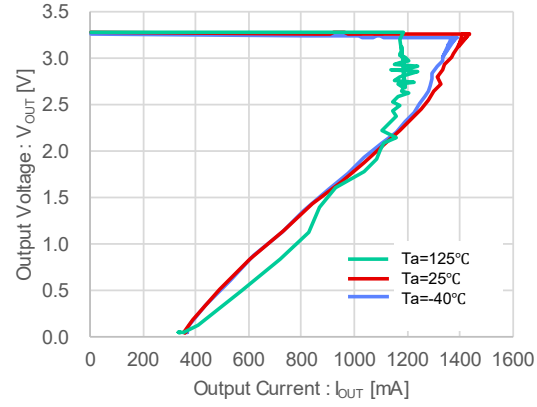
(14) High Side Current Limit vs. Ambient temperture



(15) Current Limit Operation

V_{IN}=24V, V_{OUTSET}=3.3V

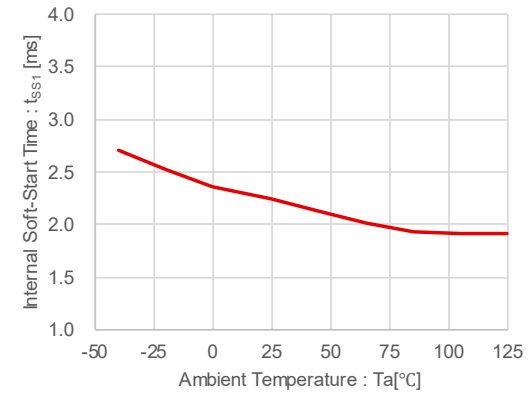
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



■TYPICAL PERFORMANCE CHARACTERISTICS

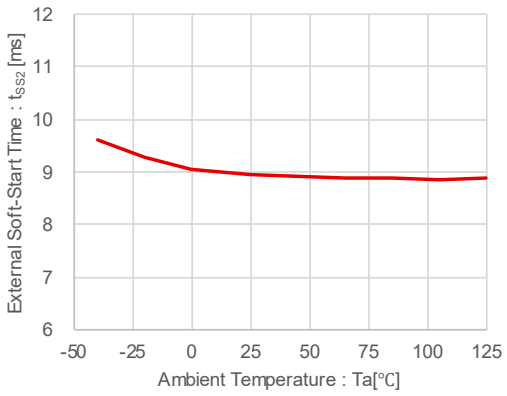
(16) Internal Soft-Start Time vs. Ambient temperature

$V_{EN/SS}$=24.0V

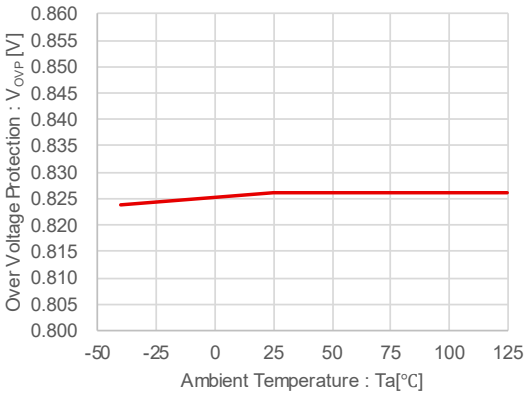


(17) External Soft-Start Time vs. Ambient temperature

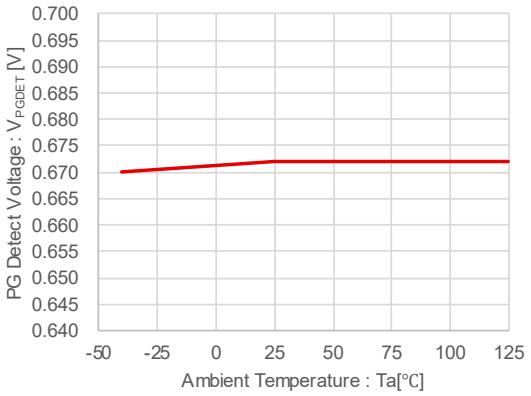
$V_{EN/SS}$=24.0V, R_{SS}=390kΩ, C_{SS}=0.47μF



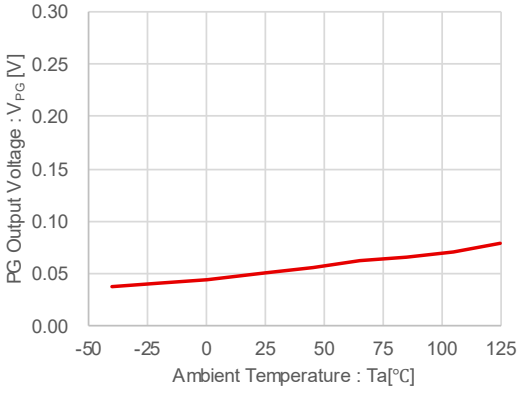
(18) Over Voltage Protection vs. Ambient Teperature



(19) PG Detect Voltage vs. Ambient Teperature

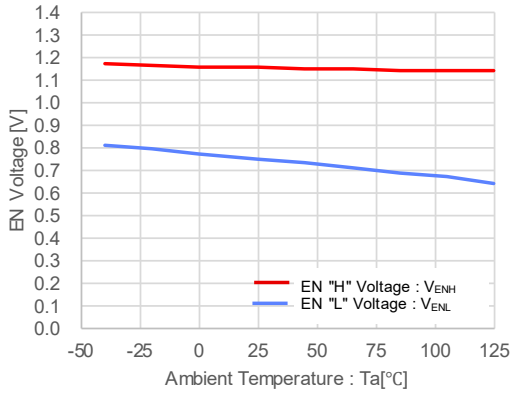


(20) PG Output Voltage vs. Ambient Teperature



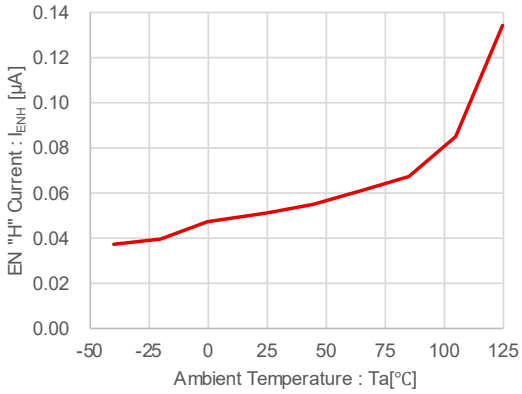
■TYPICAL PERFORMANCE CHARACTERISTICS

(21) EN Voltage vs. Ambient Temperature

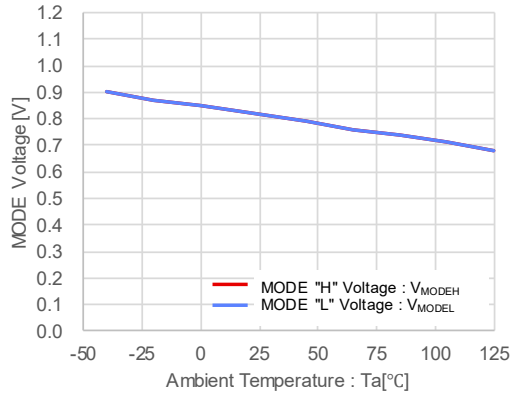


(22) EN "H" Current vs. Ambient temperture

$V_{EN/SS}$=60V

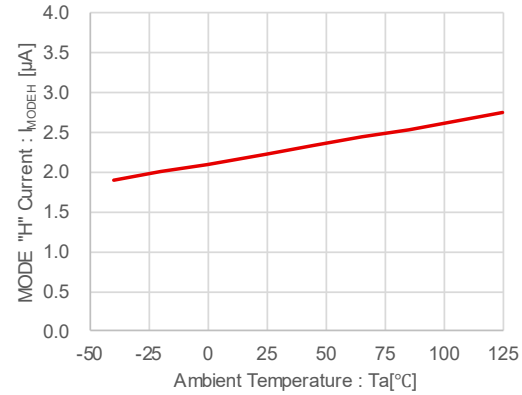


(23) MODE Voltage vs. Ambient Temperature



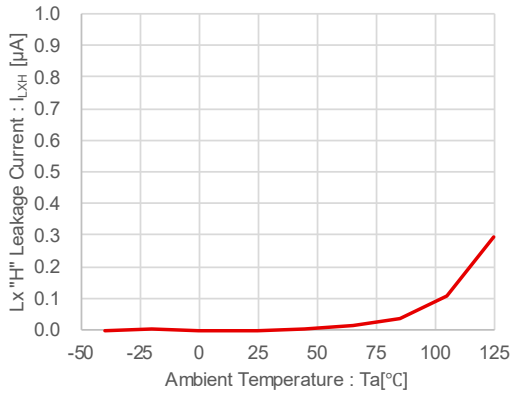
(24) MODE "H" Current vs. Ambient temperture

V_{MODE}=5.0V



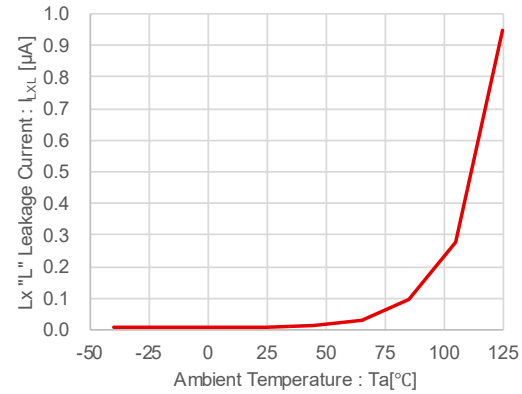
(25) Lx "H" Leakage Current vs. Ambient temperture

V_{IN}=60V, V_{LX}=0V



(26) Lx "L" Leakage Current vs. Ambient temperture

V_{IN}=60V, V_{LX}=60V

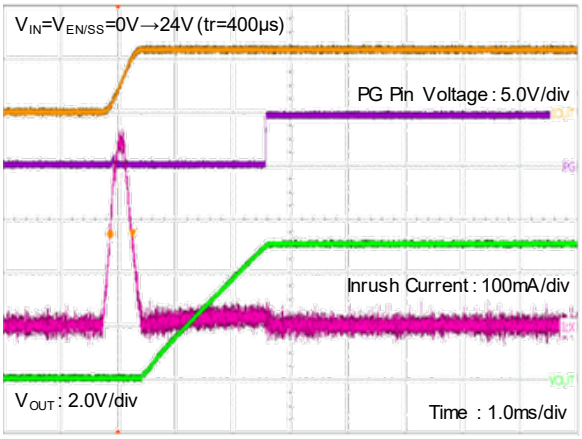


■TYPICAL PERFORMANCE CHARACTERISTICS

(27) Start-up Waveform (V_{IN} Rising)

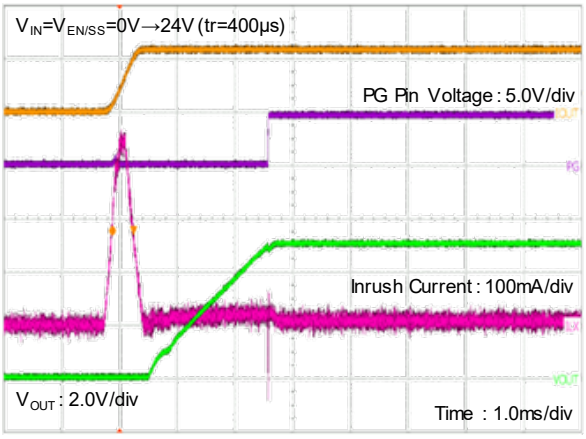
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=5.0V,R_{LOAD}=5kΩ
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



MODE="H" (PWM)

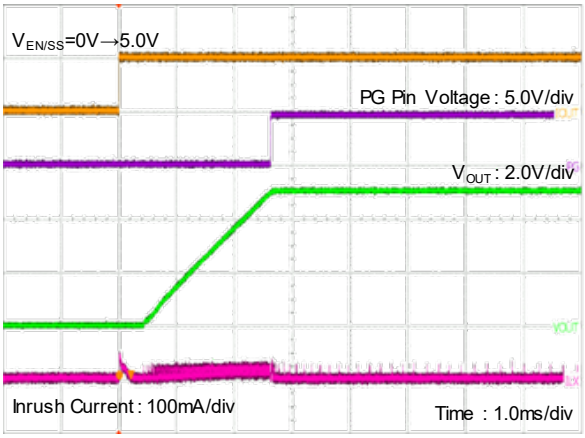
V_{IN}=24V,V_{OUTSET}=5.0V,R_{LOAD}=5kΩ
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



(28) Start-up Waveform (EN/SS Rising)

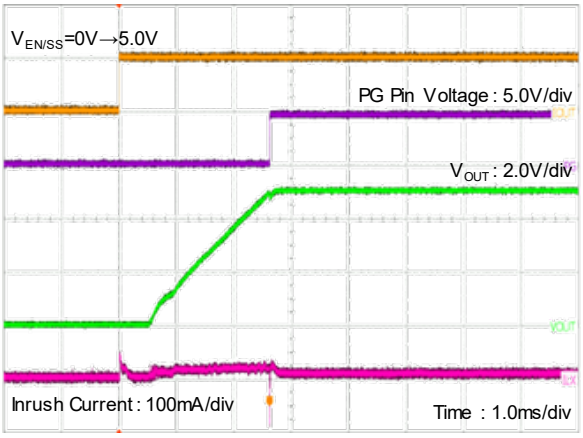
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=5.0V,R_{LOAD}=5kΩ
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



MODE="H" (PWM)

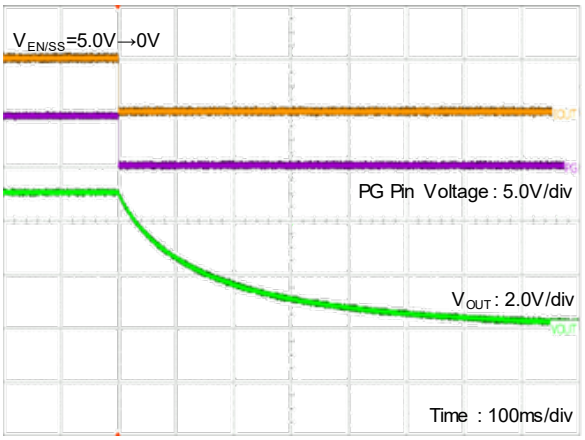
V_{IN}=24V,V_{OUTSET}=5.0V,R_{LOAD}=5kΩ
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



(29) Shutdown Waveform (EN/SS Falling)

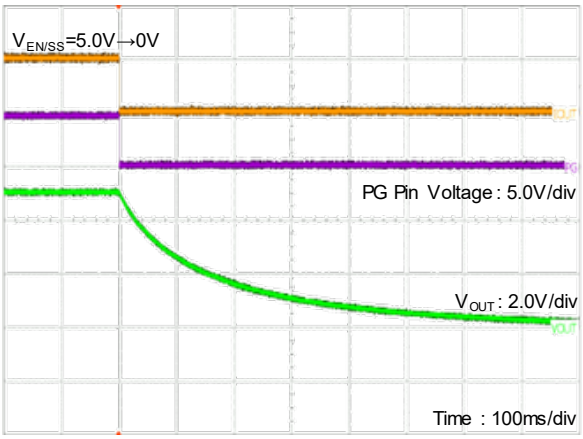
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=5.0V,R_{LOAD}=5kΩ
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=5.0V,R_{LOAD}=5kΩ
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)

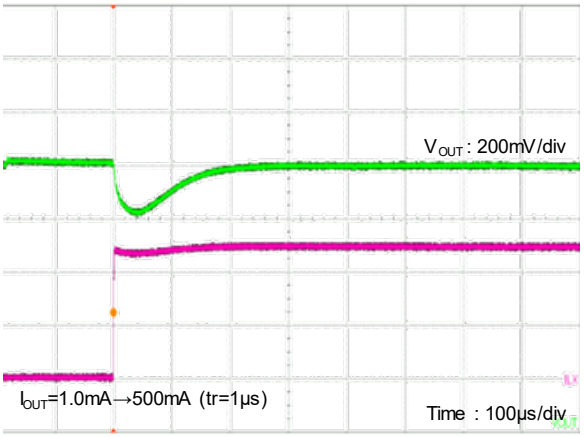


■TYPICAL PERFORMANCE CHARACTERISTICS

(30-1) Load Transient Response

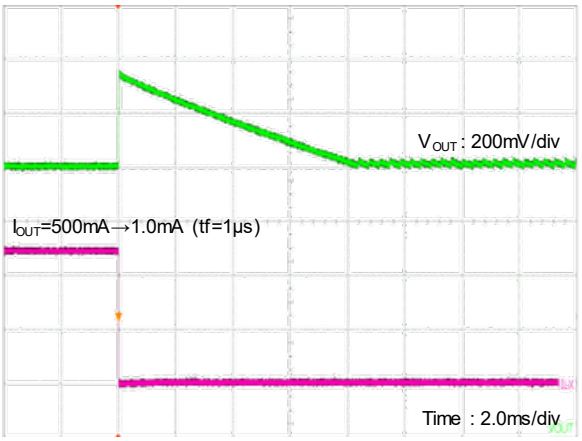
MODE="L" (PWM/PFM)

V_{IN}=12V,V_{OUTSET}=3.3V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



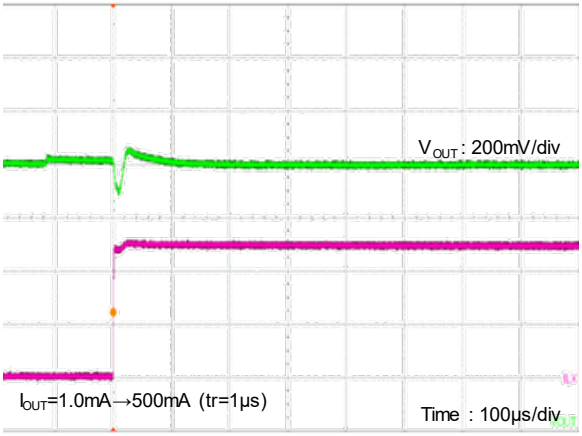
MODE="L" (PWM/PFM)

V_{IN}=12V,V_{OUTSET}=3.3V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



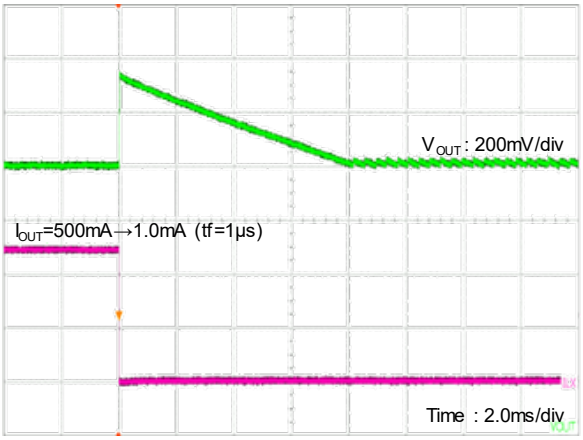
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=3.3V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



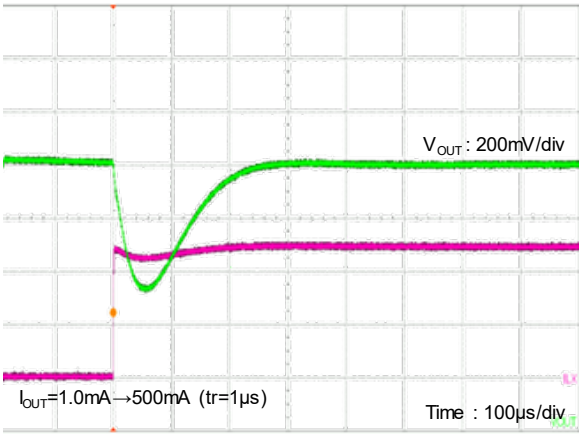
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=3.3V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



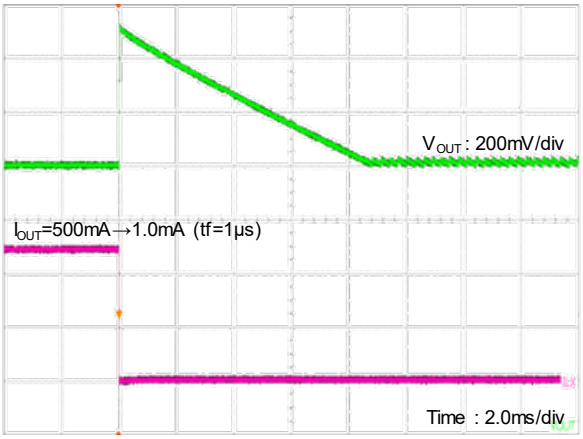
MODE="L" (PWM/PFM)

V_{IN}=12V,V_{OUTSET}=5.0V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



MODE="L" (PWM/PFM)

V_{IN}=12V,V_{OUTSET}=5.0V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)

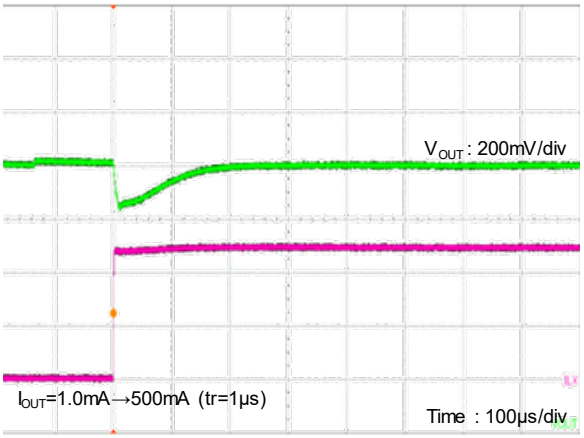


■TYPICAL PERFORMANCE CHARACTERISTICS

(30-2) Load Transient Response

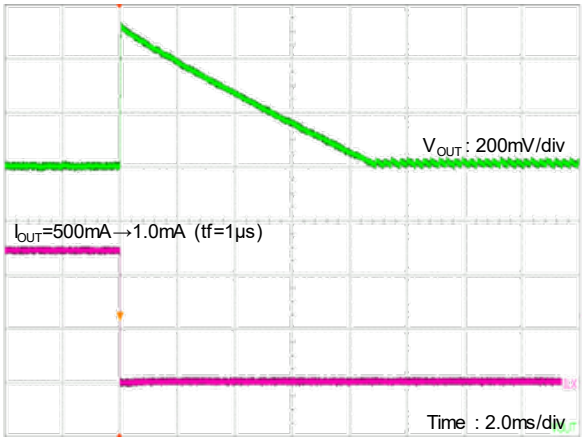
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=5.0V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



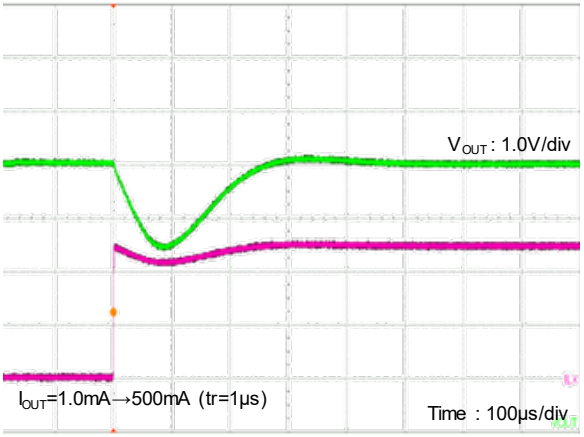
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=5.0V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



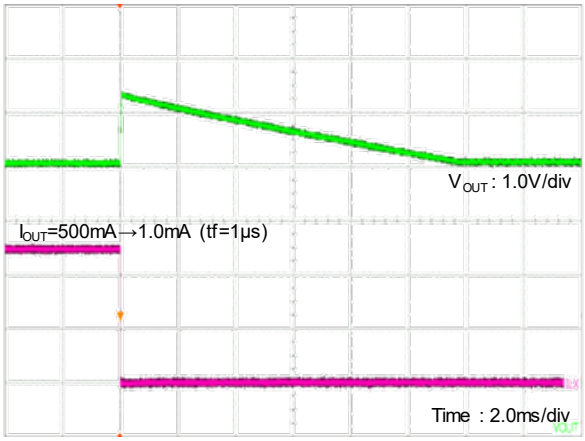
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=12V
L = 22μH(VLS5045EX-220M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 30μF(C2012X7S1E106KT x 3)



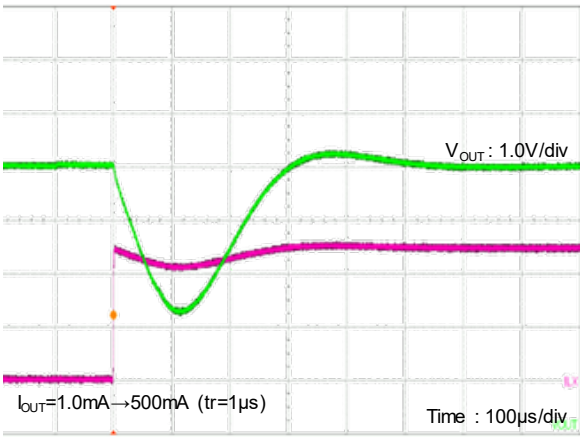
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=12V
L = 22μH(VLS5045EX-220M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 30μF(C2012X7S1E106KT x 3)



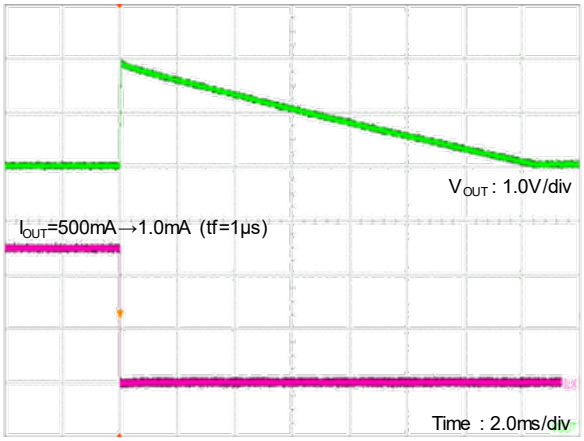
MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=18V
L = 33μH(VLS6045EX-330M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 20μF(C3216X7R1H106K160AC x 2)



MODE="L" (PWM/PFM)

V_{IN}=24V,V_{OUTSET}=18V
L = 33μH(VLS6045EX-330M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 20μF(C3216X7R1H106K160AC x 2)

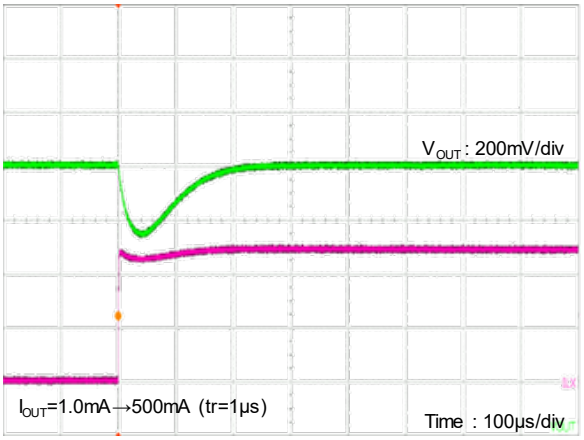


■TYPICAL PERFORMANCE CHARACTERISTICS

(30-3) Load Transient Response

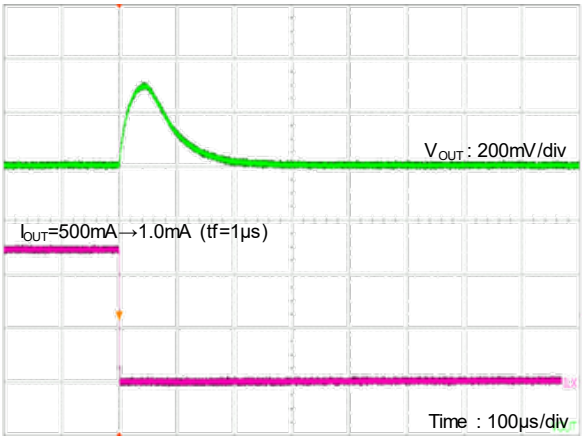
MODE="H" (PWM)

V_{IN}=12V,V_{OUTSET}=3.3V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



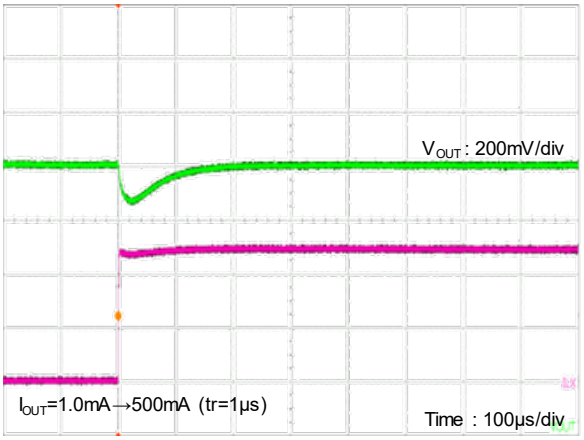
MODE="H" (PWM)

V_{IN}=12V,V_{OUTSET}=3.3V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



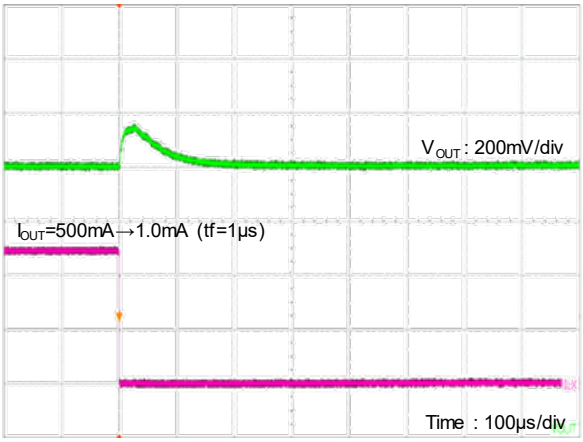
MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=3.3V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



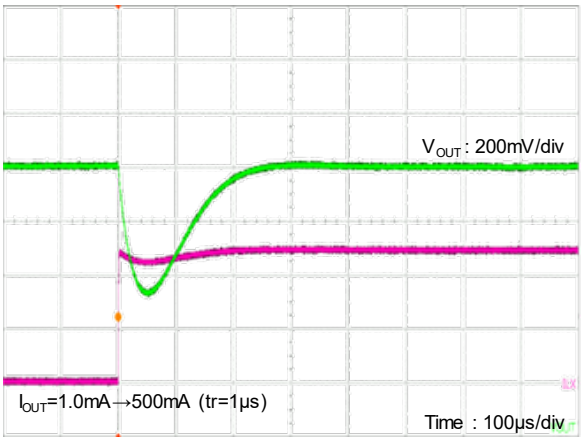
MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=3.3V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



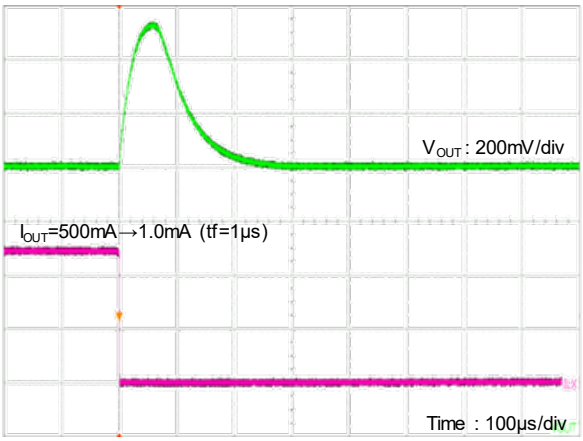
MODE="H" (PWM)

V_{IN}=12V,V_{OUTSET}=5.0V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



MODE="H" (PWM)

V_{IN}=12V,V_{OUTSET}=5.0V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)

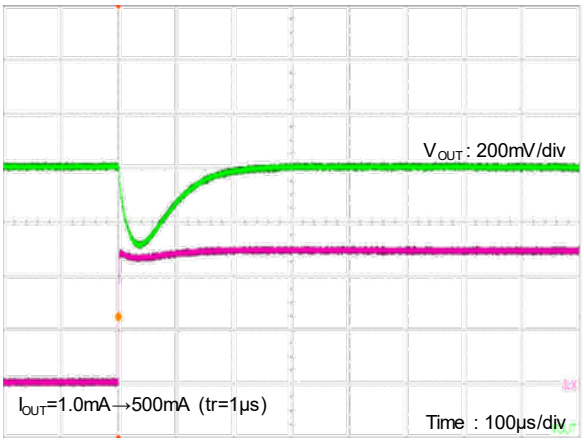


■TYPICAL PERFORMANCE CHARACTERISTICS

(30-4) Load Transient Response

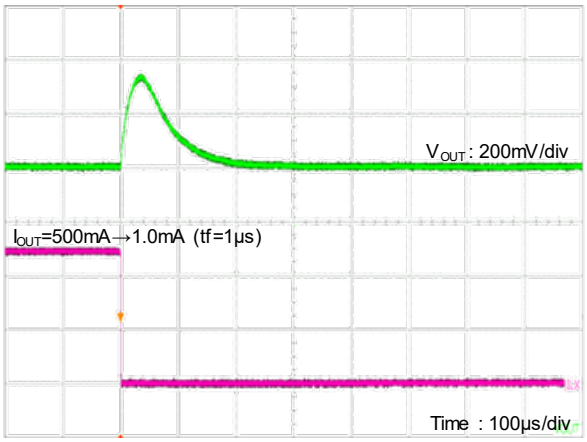
MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=5.0V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



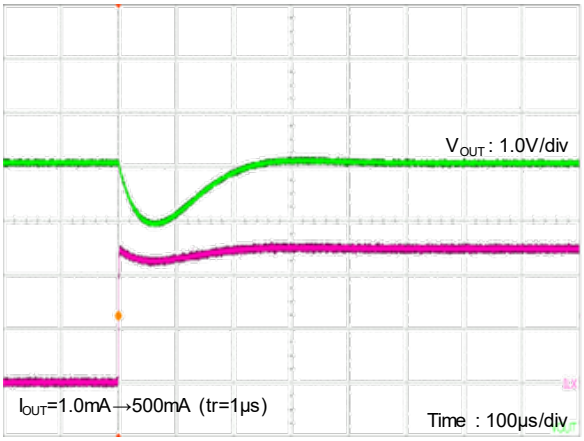
MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=5.0V
L = 10μH(VLS5030EX-100M-D)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 44μF(GRM21BD71A226ME44L x 2)



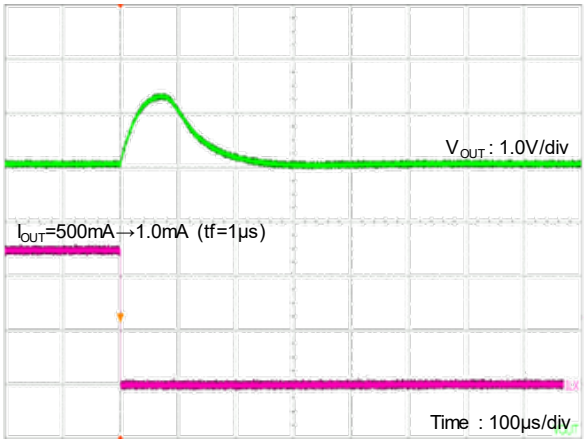
MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=12V
L = 22μH(VLS5045EX-220M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 30μF(C2012X7S1E106KT x 3)



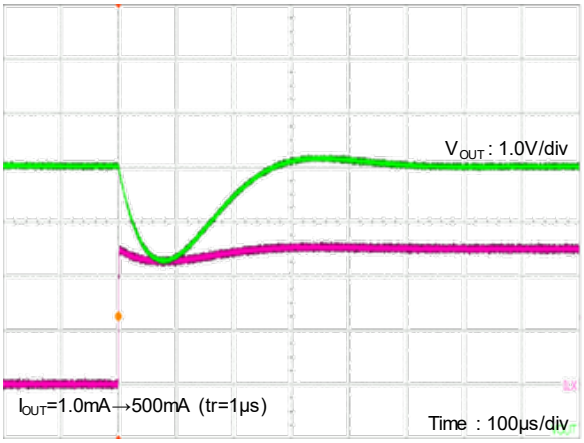
MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=12V
L = 22μH(VLS5045EX-220M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 30μF(C2012X7S1E106KT x 3)



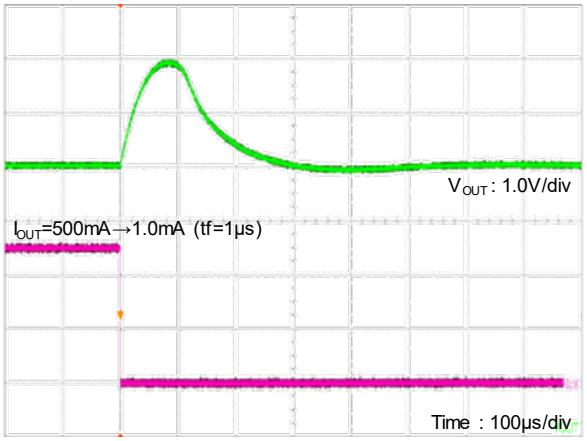
MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=18V
L = 33μH(VLS6045EX-330M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 20μF(C3216X7R1H106K160AC x 2)



MODE="H" (PWM)

V_{IN}=24V,V_{OUTSET}=18V
L = 33μH(VLS6045EX-330M-H)
C_{IN} = 4.7μF(GCM32DC72A475KE02L)
C_L = 20μF(C3216X7R1H106K160AC x 2)



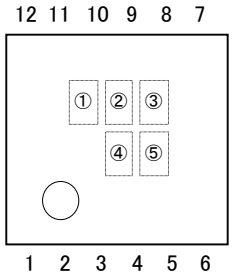
■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

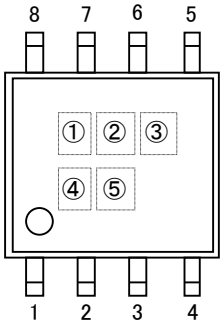
PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
DFN3030-12A	DFN3030-12A PKG	DFN3030-12A Power Dissipation
HSOP-8N	HSOP-8N PKG	HSOP-8N Power Dissipation

■MARKING RULE

DFN3030-12A



HSOP-8N



① represents products series

MARK	PRODUCT SERIES
1	XC9711******-G

② represents FB Voltage

MARK	VFB(V)	PRODUCT SERIES
0	0.75	XC9711A75***-G

③ represents Oscillation Frequency

MARK	Oscillation Frequency(kHz)	PRODUCT SERIES
1	800	XC9711***8**-G

④⑤ represents production lot number

01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order. (G, I, J, O, Q, W excluded)

* No character inversion used.

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