Torex...Powerfully Small!

RESET ICs for Consumer and Industrial Equipment

Product Overview

January 2026

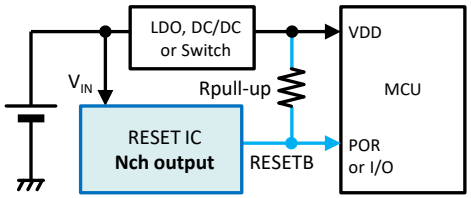
TOREX Semiconductor

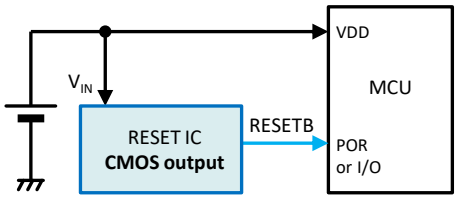
Rev. 2.0

Types of Reset ICs and Basic Circuits

Basic functions and circuits of RESET ICs

Simple function (monitored by V_{IN}) type : Nch vs CMOS output

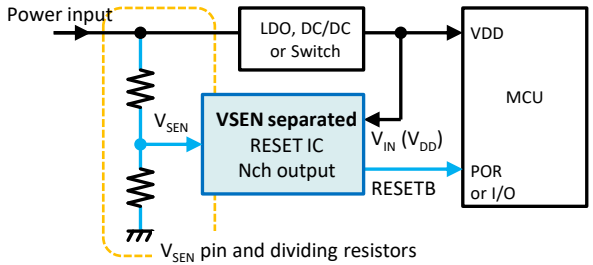




XC61CC/XC61GC, XC6126C, XC6136C　　XC61CN/XC61GN, XC6126N, XC6136N

- **If "V_{IN}" ≠ "VDD of MCU",** select **Nch open drain output,** and if **"V_{IN}" = "VDD of MCU"**, **CMOS output** can be used.
- **Nch** : When RESETB output is "H", the voltage level is shifted by a **pull-up resistor (Rpull-up)** to match the VDD of MCU.
- **CMOS** : Rpull-up is not required. No current consumption for resistor, preferred for battery monitoring.

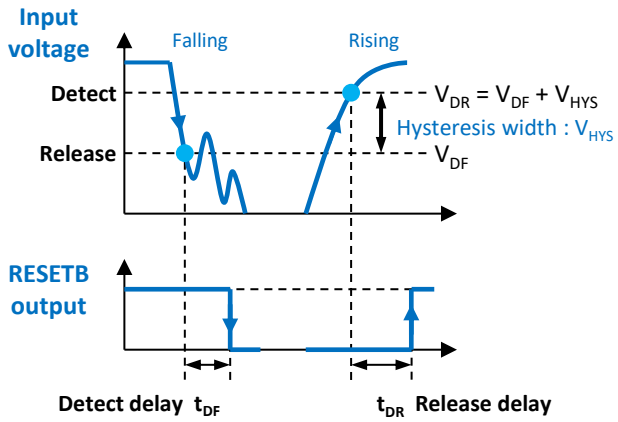
Separated V_{SEN} (sense) pin type



XC6118, XC6135, XC6132/XC6133/XC6134
XC6138 : No dividing resistors for monitoring ~76V high voltage lines

- If the power supply V_{IN} (V_{DD}), and the monitored line are different, or if a medium and high voltage line is monitored with dividing resistors.
- If V_{IN} (V_{DD}) is supplied from another line, the reset IC detects and operates normally even if the monitored V_{SEN} pin is 0V.

Appendix : Basic operation of Reset IC



Detect voltage (V_{DF})
Voltage to detect voltage drop. RESETB output goes to "L". ※

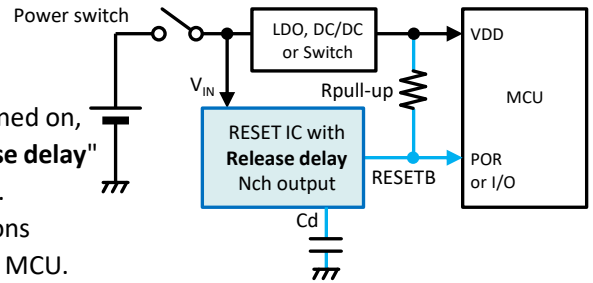
Release voltage (V_{DR})
Voltage to release when rising. RESETB output goes to "H". ※

Hysteresis width (V_{HYS})
Voltage difference of V_{DR} - V_{DF}. Generally, 5% of V_{DF}

Release/Detect delay (t_{DF}/t_{DR})
Delay between Release/Detect and RESETB change.

※ Detect (Active) "L" output type.

Release/Detect delay



- Example : Release Delay

  After the power switch is turned on, RESETB is held "L" by "**Release delay**" until MCU's VDD is stabilized. Once stable, RESETB transitions from "L" to "H", enabling the MCU. External adjustment with Cd or internally fixed type.

  (Cd: **XC6118**, **XC6119**, **XC6132/XC6133/XC6134**, **XC6138**, Fixed: **XC6127)**

- Detect delay (Cd: **XC6132/XC6133/XC6134**, **XC6138**)

  See waveform at voltage falling. This function avoids false detection caused by short undershoots.

Hysteresis width (Difference Between Detect and Release Voltage)

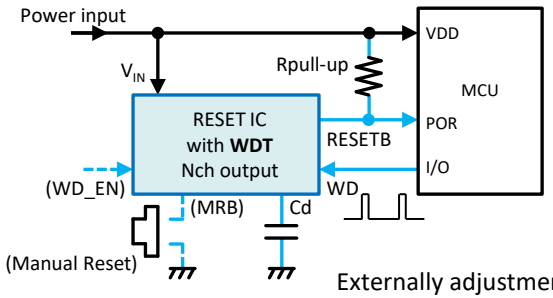
- General hysteresis width: Typically 5% of detect voltage (V_{DF}) or a few to ~10mV.
- In some cases, a wide hysteresis width is used to ensure stable system operation.

  Hysteresis width adjustable with external resistors : **XC6132/XC6134**
  Selectable wide hysteresis width from pre-programed values : **XC6138**

Types of Reset ICs and Basic Circuits : Freeze Countermeasures

■ Watchdog timer (WDT), MR function

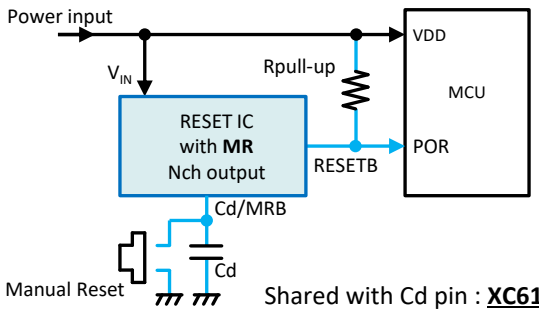
● RESET ICs with WDT function



Externally adjustment with Cd : **XC6130**, **XC6131**
Internally fixed : **XC6121/XC6122/XC6123/XC6124**

- If **no pulses come from MCU to WD pin** periodically, it is judged as a system freeze and a reset is output. A low-voltage detect function is also available.
- **WD timeout time and Detect delay** can be set externally by Cd or set internally.
- WDT EN (enable) and MR function (**XC6130**) are also available as options.

● Manual Reset (MR) function

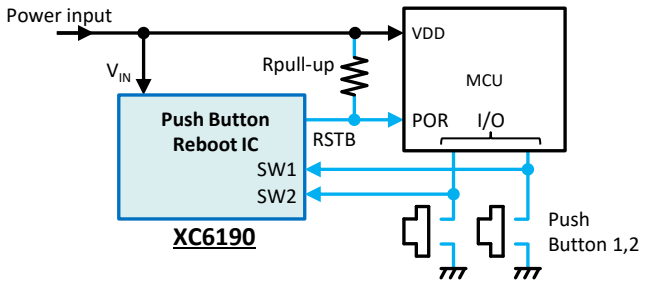


Shared with Cd pin : **XC6138**, **XC6132/XC6133/XC6134**
Dedicated pin for MR : **XC6127**, **XC6130**

- Forced reset output by "L" signal to **MRB pin.**
- Generally shared with Cd pin. Some products have a dedicated pin.

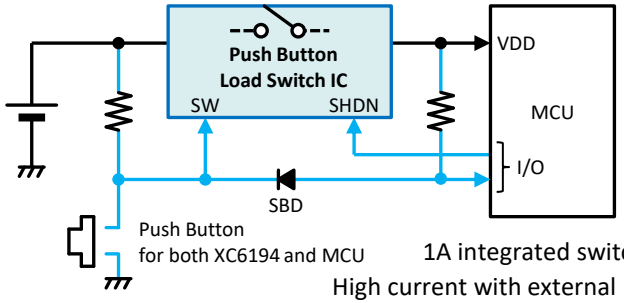
■ IC with special forced reset function

● Push Button Reboot controller



- Forced reset output **by pressing and holding one or two push buttons**.
- Push button switches for system (MCU) control can be shared. No additional switches are required.

● Push Button Load Switch



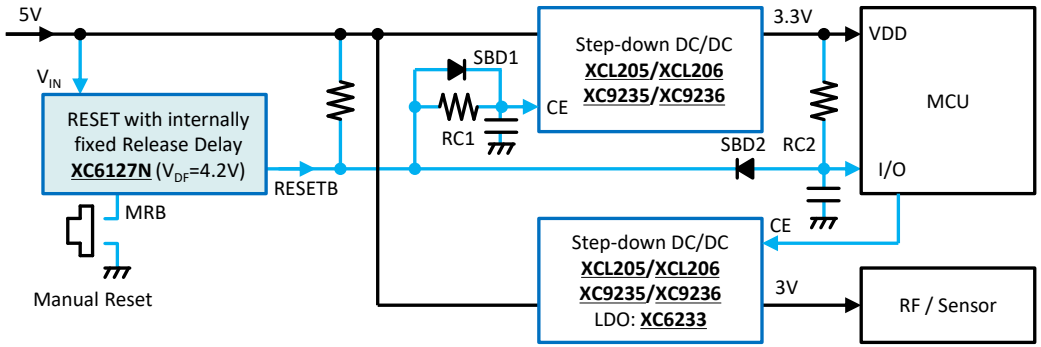
1A integrated switch : **XC6194A**
High current with external FET : **XC6193A**

- For the cutoff (Ship) switch to prevent battery discharge during shipment of battery powered and low consumption products, and for the main power switch.
- Startup is performed by pressing a push button, and shutdown is triggered by a signal from the MCU to the SHDN pin.
- An option is available to **cut off power by pressing and holding the push button**. Forced OFF by pressing and holding is possible in the event of a system freeze.

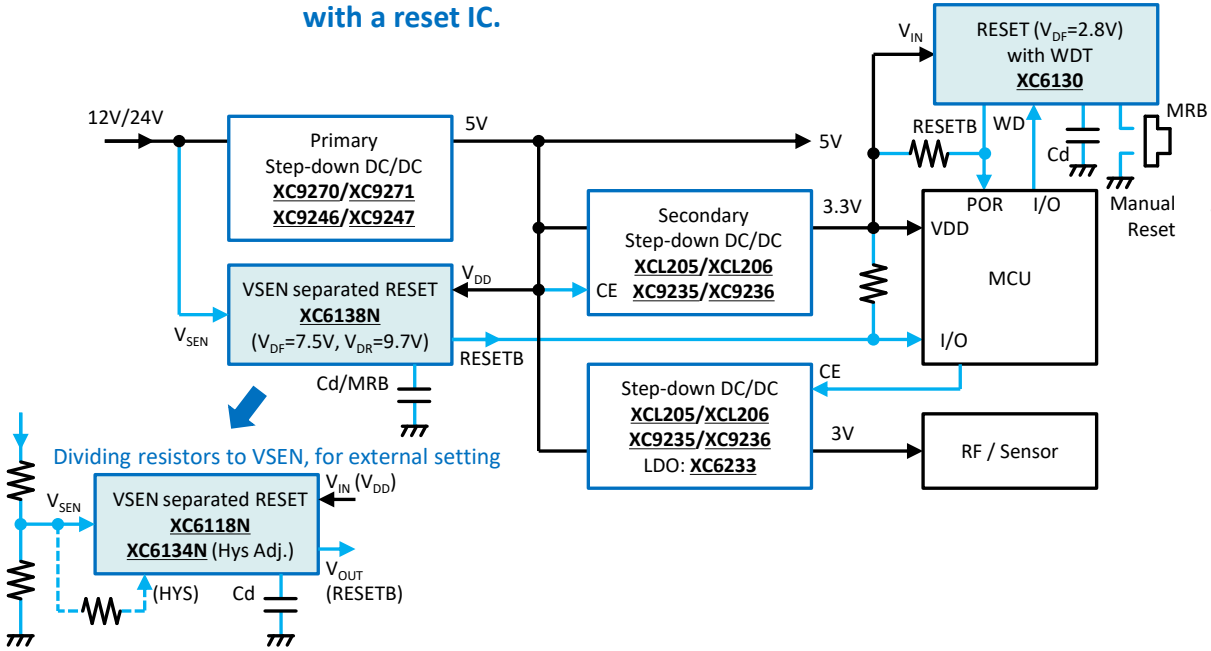
Start-up Control and Voltage Drop Monitoring for 5V/12V/24V Input Systems

■ Monitoring power lines and managing system startup, safe shutdown, and power-on/off sequences.

● 5V input: Circuit that controls the power supply and system with a reset IC



● 12V/24V input: Circuit for safe system shutdown and freeze measures with a reset IC.



Power supply start-up

- **XC6127** with the release delay waits for 5V line to stabilize after rising, then releases and starts the CE of DC/DC through **SBD1**.
- Wait for DC/DC startup with **RC2** delay, then start MCU.

Safe system shutdown / Power down

- When **XC6127** detects a voltage drop, it communicates through **SBD2** to MCU I/O, then **MCU executes the shutdown program**.
- Then shut down DC/DC after **RC1** delay.

Freeze measures

- Resolved by **Manual Reset function** of **XC6127**.

Power supply start-up

- MCU starts up after the release delay of **XC6138**.
- If RESET with WDT **XC6130** is also provided, monitor the power supply of MCU and start it after its release delay.

Safe system shutdown / Power down

- When 12V/24V drops and **XC6138** detects it, it tells the MCU I/O before 5V drops and the **MCU executes the shutdown program**.
- The secondarily DC/DC continues to operate after 5V input begins to drop and maintains power until the MCU shutdown.

Freeze measures

- **XC6130** monitors 3.3V line and automatically restarts MCU by detecting system freezes and resetting it with **WDT function**. **Manual Reset function** is also available.

Appendix : Monitoring with Wide Detect/Release Voltage Difference on 12V/24V Lines

■ A method for monitoring and controlling power supply lines with large fluctuations, caused by impedance or loads such as motors, in 12V/24V devices, using a large detect/release voltage difference.

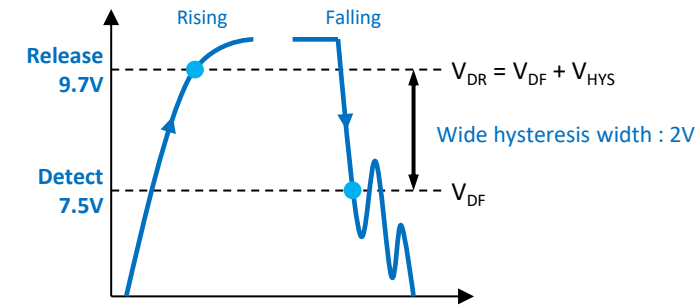
Challenges

- In the normal 5% hysteresis width, detect/release is repeated due to voltage fluctuation.
- At startup, release should be made after sufficient voltage has risen.
- and should operate over a wide input voltage range down to sufficiently low voltages.

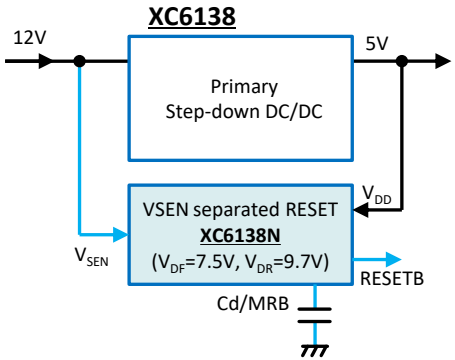
Measures

- Use a reset IC with a large detect and release voltage difference (Hysteresis width).

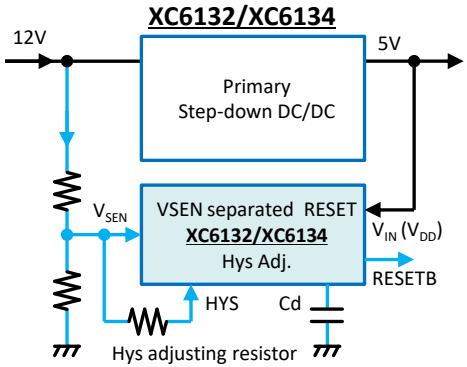
12V input waveform and voltage



Pre-programed wide hysteresis width



Hysteresis width set by an external resistor



XC6138 : Example of internal set voltages for 12V/24V lines

Both 5% and 30% hysteresis widths are available for various applications.

Monitored line	Detect voltage	Release voltage	Hys	note
12V line	9.5V	10.0V	5.3%	12V monitoring, Hys: 5%
	7.5V	**9.7V**	**29.3%**	**12V monitoring, Wide Hys**
24V line	19.0V	20.0V	5.3%	24V monitoring, Hys: 5%
	15.5V	**20.0V**	**29.0%**	**24V monitoring, Wide Hys**

Concept of detect/release voltage difference

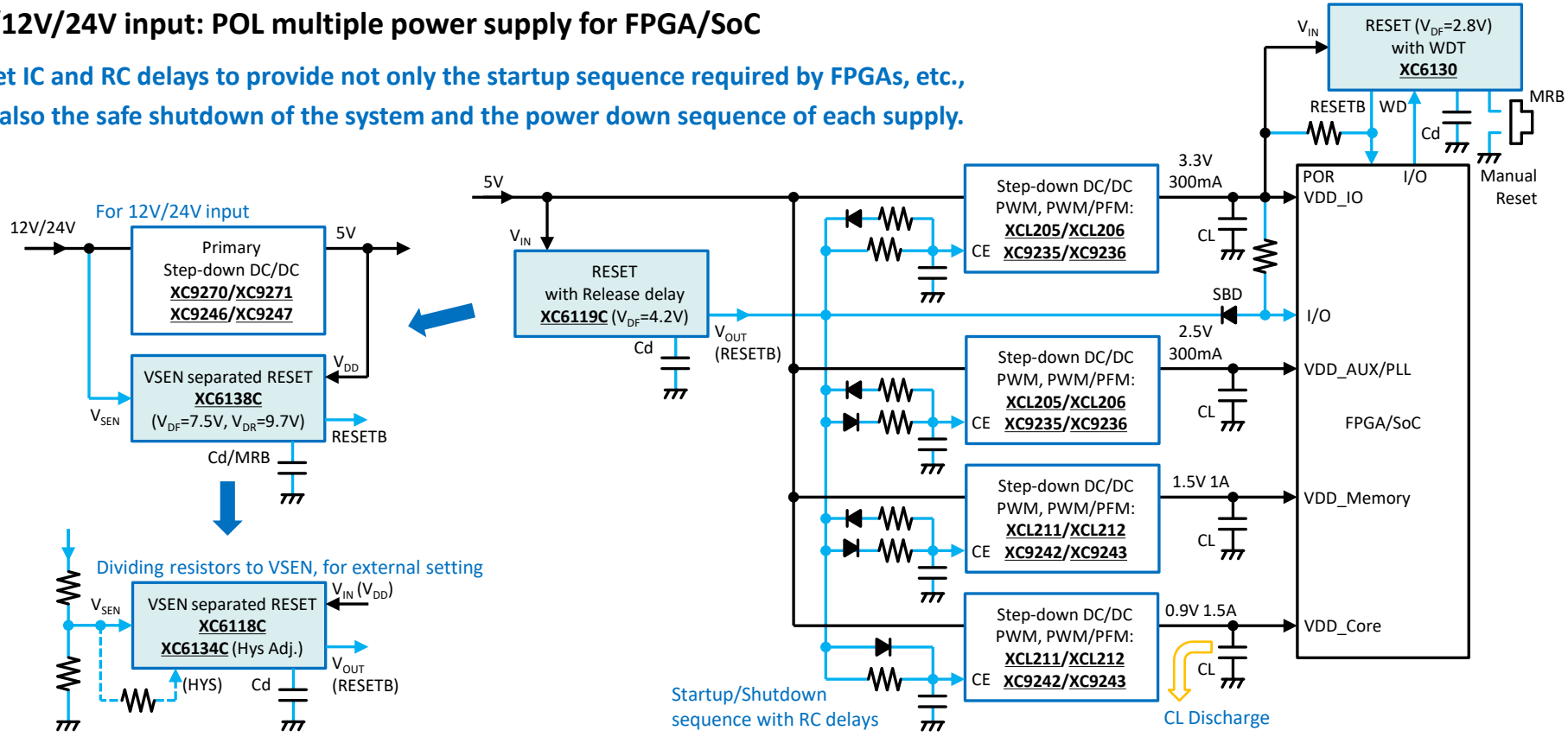
- **Detect** : The voltage should be 80% or 90% of 12V or 24V.
  Assume that the input voltage may rise slowly and wait for stability with a release delay.
- **Release** : Select a voltage at which operation is still sufficiently stable, e.g., 7V or higher if the output voltage of the primary DC/DC is 5V.
  Also, provide a sufficient difference of 20~30% from the detection voltage.

➢**Safe shutdown**

Notify the system (MCU) of detection to execute the shutdown sequence and stop the subsequent power supplies. (See previous and next pages)
Note that the system shutdown is completed against the falling speed of the input voltage and the output voltage of the primary DC/DC.

5V/12V/24V input: POL multiple power supply for FPGA/SoC

- **Reset IC and RC delays to provide not only the startup sequence required by FPGAs, etc., but also the safe shutdown of the system and the power down sequence of each supply.**



Power supply start-up

- **CMOS output** of RESET **XC6119 / XC6138** with the release delay drives RC delays to CE of each DC/DC.
  Starts up each DC/DC according to power-up sequence order.

Safe system shutdown / Power down

- When **XC6119 / XC6138** detects a voltage drop, it first tells the I/O of FPGA through a **SBD**, and **FPGA executes a shutdown program**.
- Then, each DC/DC is turned off according to the power down sequence order set by RC delays to CE of each DC/DC.
- Startup and power down order of each DCDC is switched by the SBD of each RC.

Freeze measures

- **XC6130** monitors 3.3V line and automatically restarts the FPGA by detecting system freezes and resetting it with **WDT function.**
- **Manual Reset function** is also available.

Appendix : Rise/Fall Sequence of Multiple Power Supplies and Countermeasures Against Loss of Power

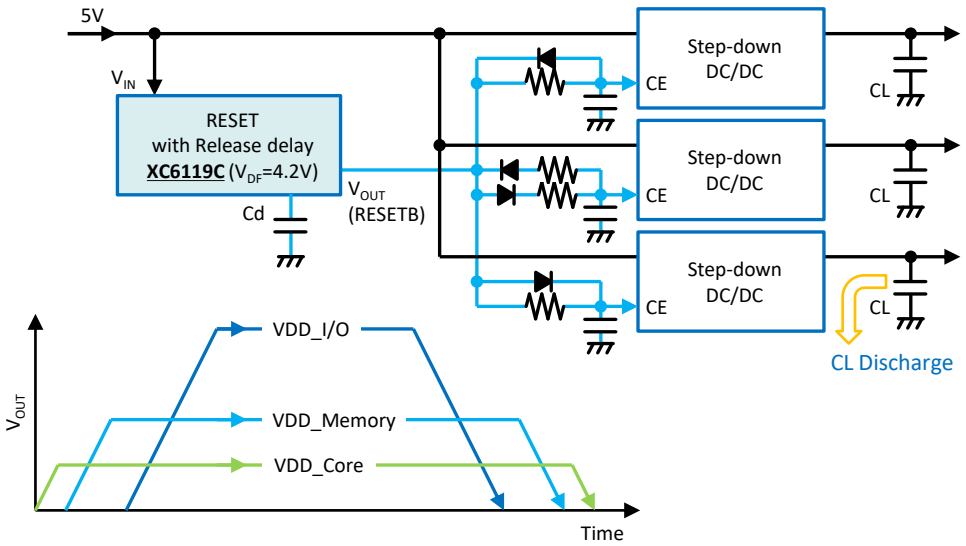
How to create a rise/fall sequence for POL multi-supply

Challenges

- The rising order of each power supply in FPGA is specified.
- Order of falling order may also be defined, which is difficult to achieve.

Measures

- Both rising/falling orders are realized by using a **reset IC and RC delays**. For falling, CL discharge function of DC/DC is used.



RC delay setting

- CMOS output of the reset IC drives the RCs.
  The delay until each DC/DC starts to turn on/off is calculated as follows

$$t_{delay(ON)} = R \times C \times (-\ln((V_{IN} - V_{CE}) / V_{IN}))$$

$$t_{delay(OFF)} = R \times C \times (-\ln(V_{CE} / V_{IN}))$$

※ V_{CE} is the threshold voltage of CE

- Set considering the soft-start time of each DC/DC and the discharge time by CL discharge.

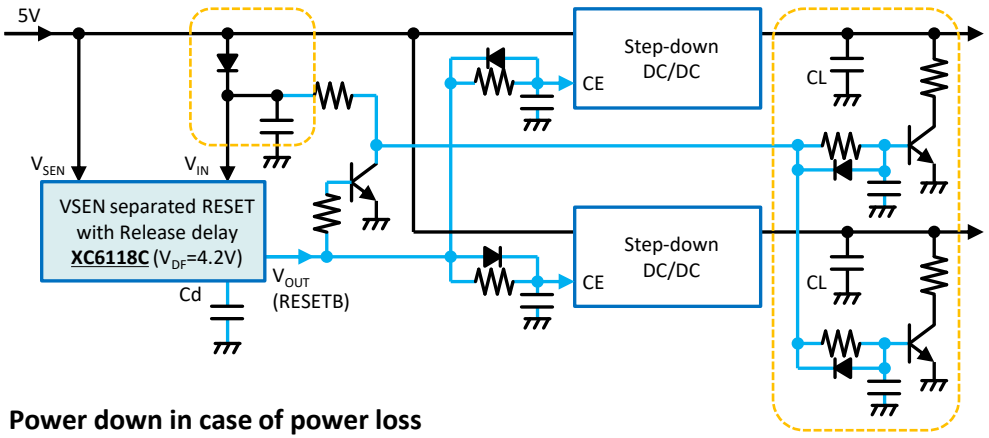
How to ensure power down in the event of power loss

Challenges

- If power is suddenly lost, the falling sequence shown at left does not work.

Measures

- A circuit that maintains the **V_{IN}(V_{DD}) voltage of V_{SEN} separated reset IC** and a **simple discrete circuit that discharges CL** enables the device to be safely shut down.



Power down in case of power loss

- **SBD and C to V_{IN} (V_{DD})** of V_{SEN} separated type ensure power supply for a while even in case of power loss.
- Even if DC/DC V_{IN} is lost, **each CL can be discharged with a simple Tr circuit**. The sequence can also be easily set up with RC on the base of Tr.
- Together with a larger CL for Core, the specified falling order is achieved.

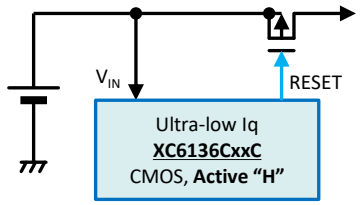
➢Adding a **Backup circuit** is also helpful.

If you need help with actual sequence studies/calculations, please contact us.

UVLO switch

Switch to cut off load when input voltage drops

- Detects a voltage drop in battery or power supply line and cuts off the Pch FET.

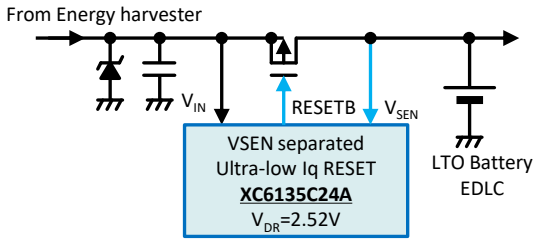


- Low consumption is especially important for battery applications.
  - Ultra-low Iq **XC6136C**, CMOS output, detect "H" type, directly drives the gate of Pch FET.

Micro-power energy harvesting charging circuit

Ultra-low Iq charge control for micro power such as rectenna output

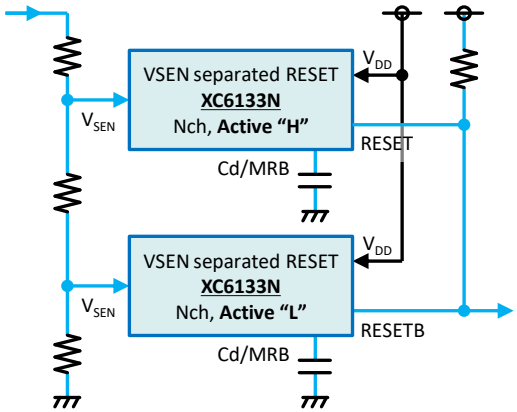
- Ultra-low Iq reset **XC6135C** enables a charge control circuit with current consumption small enough for several µW power such as rectenna.
  - If the LTO battery or EDLC is below the release voltage and the operating voltage is applied to V_{IN} from an energy harvest, Pch FET is turned on.



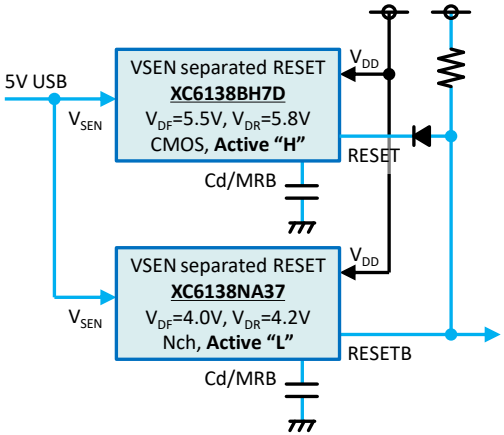
Window comparator

Outputs "L" outside the set two voltages

- Detect (active) "H" and "L" types are used for overvoltage detection (OVP) and undervoltage detection (UVLO), respectively.
- Two N-channel open drain outputs with OR Connection.



- **XC6138** has a standard product suitable for OVP and UVLO for 5V line. However, since the product for OVP has CMOS output, SBD is inserted.



RESET IC, Watchdog Timer (RESET/WDT) : Feature

■ Voltage Detector & Watchdog Timer

- Ultra-small / Ultra-Low Quiescent Current for Extended Battery Life / Separated Sense Pin for Medium and High voltage detection
- Detection / Release Delay, Manual Reset (MR), Output Logic “H” or “L”, Watchdog Function

➢ Voltage Detector (RESET IC)

Simple type

XC6136	
Iq=88nA ±0.8% RESETB/RESET	Ultra-Low Iq High accuracy

XC61C/G	
10V Iq=0.7μA	10V operation

Delay function

XC6119	
Iq=0.9μA	Externally adjustable release delay

XC6127	
Iq=0.7μA ±0.8% RESETB/RESET MR	Fixed release delay (50~800ms) High accuracy

Separated sense pin (V_{SEN})

XC6135	
Iq=44nA ±0.8% RESETB/RESET	Ultra-Low Iq High accuracy

XC6118	
Iq=0.8μA ±2.0%	Externally adjustable release delay

Separated sense pin (V_{SEN}) Multi-function

XC6132/XC6133/XC6134	
Iq=1.28μA, ±1.2% RESETB/RESET MR, 125℃	Hysteresis external adj. (XC6132/34) Detect/Release delay external adj. Serge protection (XC6132)

XC6138	
VSEN 76V Iq=0.5μA I_{SEN}: 0.15μA RESETB/RESET MR, 125℃	Built-in divider resistor Selectable hys: 5–50% Detect/Release Delay external Adj.

➢ Watchdog Timer(WDT) + Voltage Detector

WDT/Delay externally adjustable

XC6130/XC6131	
Iq=9.8μA ±1.0% 125℃	WDT/Delay external adj. WDT EN/ENB (XC6131) MR (XC6130)

WDT/Delay Internally fixed

XC6121/XC6122/XC6123/XC6124	
Iq=10μA	WDT/delay internally fixed WDT EN/ENB

UNDER DEVELOPMENT

XC6181/XC6182/XC6183/XC6184	
Iq=6.6μA 1.5% 125℃	WDT/delay internally fixed WDT EN/ENB

Window WDT WDT/Delay Internally fixed

UNDER DEVELOPMENT

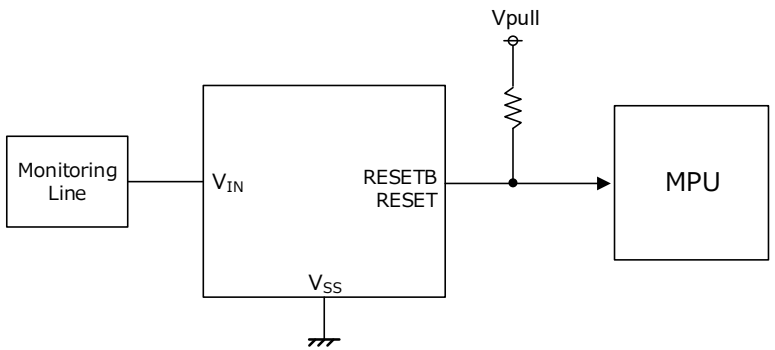
XC6185/XC6186/XC6187/XC6188	
Iq=6.6μA 1.5% 125℃	Window WDT WDT/delay internally fixed WDT EN/ENB

Ultra-Low Power / High Accuracy / Ultra Small

Features

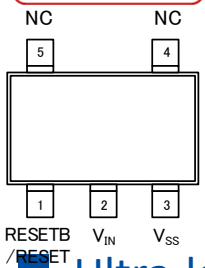
Operating Voltage	: 1.1V ~ 6.0V (Absolute Max.:7.0V)
Detection Holding Voltage	: 0.4V ~ @ CMOS 0.79V(V_{UVLOD}) ~ @ Nch Open Drain
Detect Voltage Range	: 1.2V ~ 5.0V (0.1V increments)
Accuracy	: ±0.8%
Temperature Characteristics	: ±50ppm/℃
Hysteresis width	: V_{DF}×5.0% (A/C Type) 2mV ~ 28mV (B/D Type)
Supply Current	: 88nA
Output Type	: CMOS, Nch Open drain
Output Logic	: "H" level or "L" level at detection
Function	: Undefined Operation Protection
Undefined Operation Protection	: Output Voltage 0.38V(MAX:Ta=-40℃~ 105℃)
Package	: USPQ-4B05, SSOT-24, SOT-25
Operating ambient Temp.	: -40℃ ~ 105℃

Typical Application Circuit

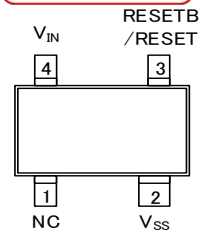


Package

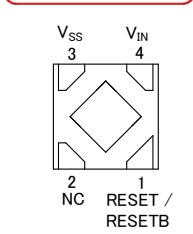
SOT-25 (2.8x2.9x1.3mm)



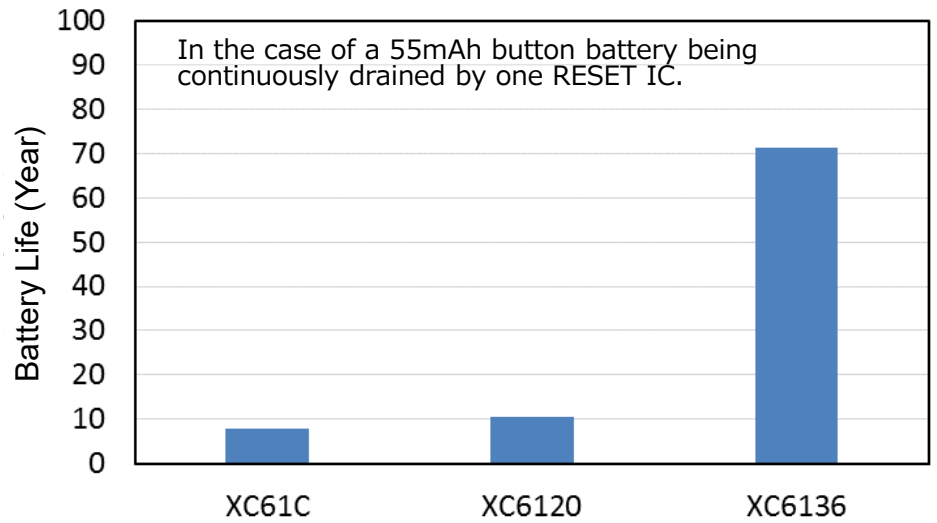
SSOT-24 (2.0x2.1x1.1mm)



USPQ-4B05 (1.0x1.0x0.33mm)



Ultra-low current consumption



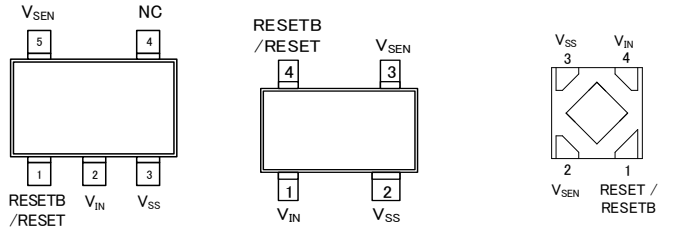
Ultra-Low Power / Separated Sense Pin / Undefined Operation Protection

Features

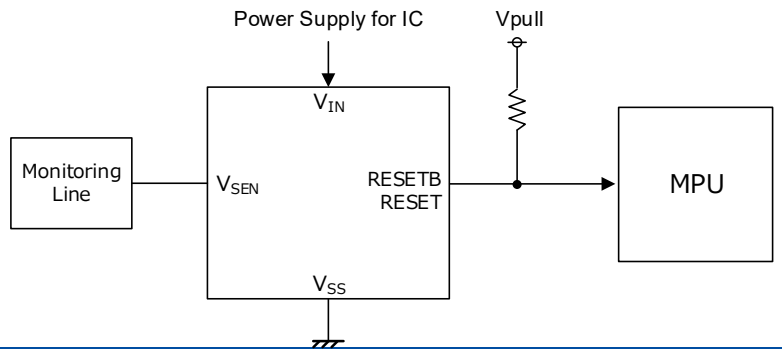
Operating Voltage	: 1.1V ~ 6.0V (Absolute Max.:7.0V)
Detect Voltage Range	: 0.5V ~ 5.0V (0.1V increments)
Accuracy	: ±0.8%
Temperature Characteristics	: ±50ppm/℃
Hysteresis width	: V_{DF}×5.0% (A/C Type) 2mV ~ 28mV (B/D Type)
Supply Current	: 53nA (@detection, V_{IN}=1.1V) 44nA (@released, V_{IN}=1.1V)
Output Type	: CMOS, Nch Open drain
Output Logic	: "H" level or "L" level at detection
Function	: Separated Sense Pin
Undefined operation Protection (CMOS Output only)	: Output pin Voltage 0.38V (MAX：Ta=-40℃~ 105℃) @V_{IN} pin ＜ Minimum operation Voltage
Package	: USPQ-4B05, SSOT-24, SOT-25
Operating ambient Temp.	: -40℃ ~ 105℃

Package

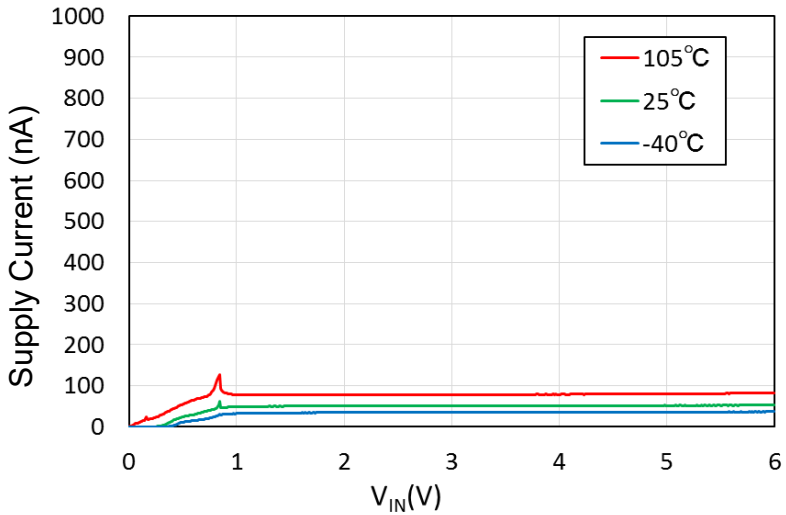
SOT-25	SSOT-24	USPQ-4B05
(2.8x2.9x1.3mm)	(2.0x2.1x1.1mm)	(1.0x1.0x0.33mm)
TOREX Longevity Program (TLP)	TOREX Longevity Program (TLP)	TOREX Longevity Program (TLP)



Typical Application Circuit



Ultra-low current consumption



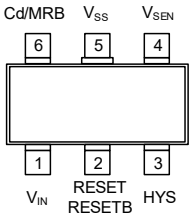
Delay Capacitor Adjustable / Surge Voltage Protection / HYS External Adjustment

Features

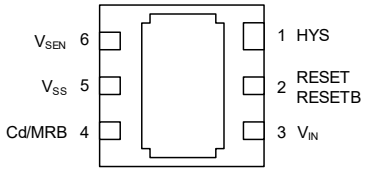
Operating Voltage	: 1.6V ~ 6.0V (Absolute Max.:7.0V)
Detect Voltage Range	: 0.8V ~ 2.0V
Detect Voltage Accuracy	: ±1.2% (Ta=25℃) ±2.7% (Ta=-40~125℃)
Temperature Characteristics	: ±50ppm/℃
Hysteresis width	: V_{DF}×0.1%
Supply Current	: 1.28μA
Function	: Separated Sense Pin/Surge Protection Manual Reset Release delay / Detection delay Adj Adj Hysteresis Width
Output Type	: CMOS, Nch Open drain
Output Logic	: "H" level or "L" level at detection
Package	: USP-6C, SOT-26
Operating Ambient Temp.	: -40℃ ~ 125℃

Package

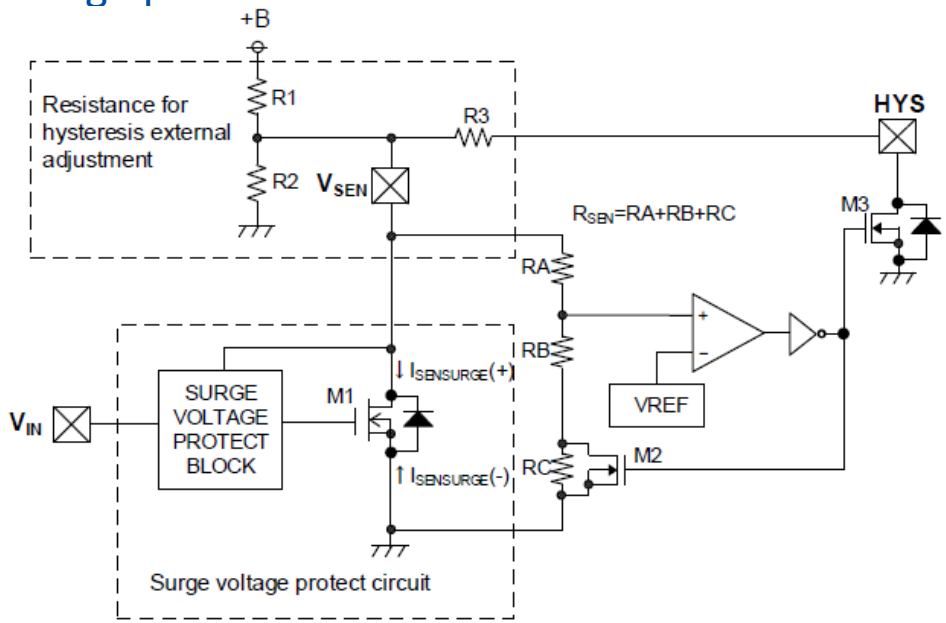
SOT-26
(2.8x2.9x1.3mm)
TOREX Longevity Program (TLP)



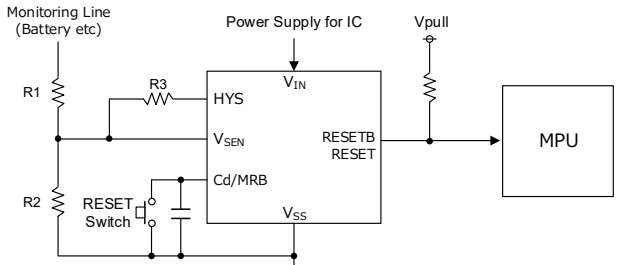
USP-6C
(1.8x2.0x0.6mm)
TOREX Longevity Program (TLP)



Surge protection function built in IC



Typical Application Circuit



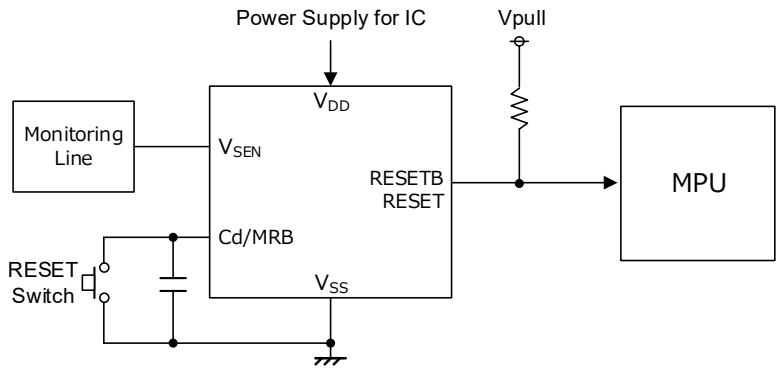
High voltage lines can be monitored and adjusted to any detect/release voltage by R1-3

Detect (VSEN) pin 76V operation / Ultra low power / Wide range of hysteresis settings

Features

Operating Voltage	: 2.2V ~ 6.0V (Absolute max.: 6.5V)
Sense Input Voltage	: 0V ~ 76.0V (Absolute max.: 80.0V)
Detect Voltage Range	: 2.3V ~ 20.0V
Release Voltage Range	: 2.5V ~ 24.0V
Accuracy	: ±1.5%(Ta=25℃), ±3.0% (Ta=-40~125℃)
Temperature Characteristics	: ±50ppm/℃
Hysteresis Range	: 5% ~ 50% (semi-custom)
Supply Current	: V_{DD}: 0.5μA, V_{SEN}: 0.15μA@12V
Output Type	: CMOS / Nch open drain
Output Logic	: "H" level or "L" level at detection
Function	: Release delay / Detection delay Adj *Detect/Release time ratio is selectable. Manual RESET Separated Sense Pin
Package	: SOT-25, DFN1515-6A
Operating Ambient Temp.	: -40 ℃ ~ 125 ℃ (Tjmax=150°C)

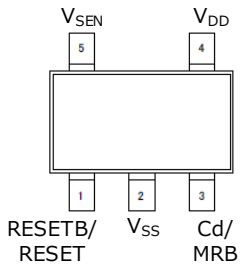
Typical Application Circuit



Package

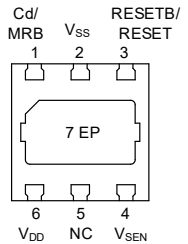
SOT-25
(2.8x2.9x1.3mm)

TOREX Longevity Program (TLP)

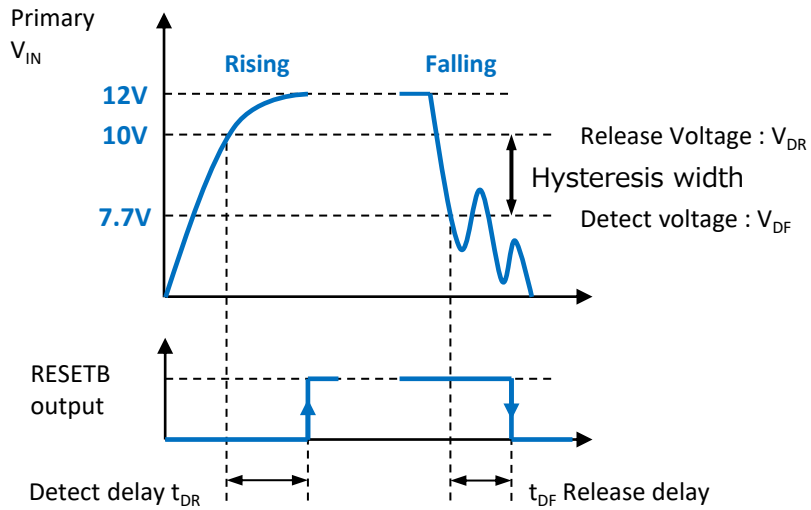


DFN1515-6A
(1.5x1.5x0.38mm)

TOREX Longevity Program (TLP)



Example of monitoring a 12V power line



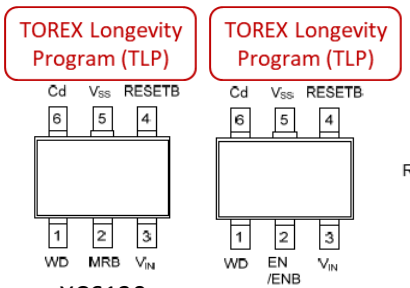
Wide Operating Temperature ~125℃ / Watchdog Function ON_OFF / Manual Reset

Features

Operating Voltage	: 1.5V ~ 6.0V (Absolute Max.:7.0V)
Detect Voltage Range	: 1.6V ~ 5.0V (±1.0% / SOT-26) 1.6V ~ 5.0V (±1.5% / DFN1515-6A)
Temperature Characteristics	: ±50ppm/℃
Hysteresis Width	: V_{DFL}×5.0%
Output Configuration	: Nch Open drain
Supply Current	: 8.1μA : Detect 9.8μA : Release 2.5μA : Release (EN=L)
WD Timeout Time	: 100ms (Cd=0.1μF)
Release Delay Time	: 100ms (Cd=0.1μF) (at power on) 10ms (Cd=0.1μF) (After Watchdog Timeout)
Function	: Manual Reset (XC6130) : Watchdog function ON/OFF (XC6131)
Package	: SOT-26, DFN1515-6A
Operating Ambient Temp.	: -40℃ ~ 125℃

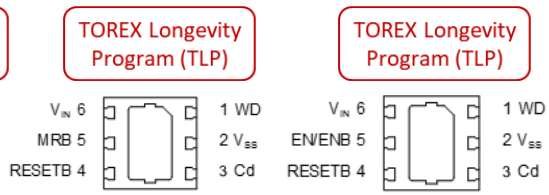
Package

SOT-26 (2.8x2.9x1.3mm)



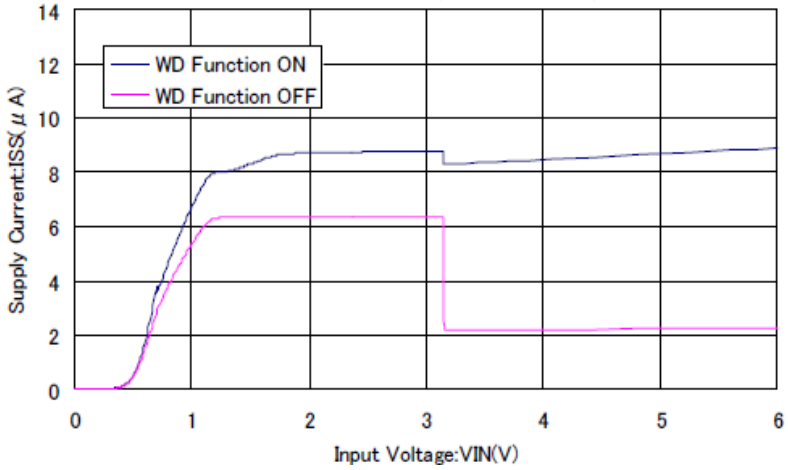
XC6130 XC6131

DFN1515-6A (1.5x1.5x0.38mm)



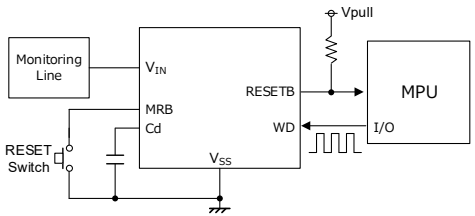
XC6130 XC6131

Watchdog function can be turned on/off

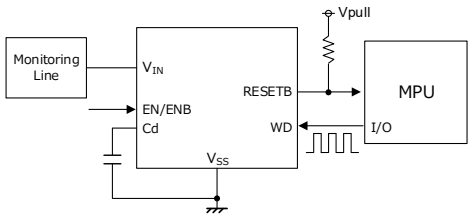


Typical Application Circuits

XC6130



XC6131



▷Low Voltage Voltage Detectors : Input Voltage/Sense pin Voltage 6V or less

Product	Feature	V_{IN} [V]	V_{DF} [V]	Accuracy	Iq [μA]	Output		Voltage Detect						Topr max.	Package ☑ : Torex Longevity Program(TLP)
						Config.	Logic	Separate Sense Pin	Detect Delay time	Release Delay time	Hys	Manual Reset	Unstable operation prevention		
XC6136	Ultra Low Power	1.1~6.0	1.2~5.0	1.0%	0.088	CMOS Nch	Detect "H" Detect "L"	-	-	-	VDFx0.1%	-	CMOS Only	105℃	☑USPQ-4B05 (1.0x1.0xh0.33mm) ☑SSOT-24 ☑SOT-25
XC6135	Ultra Low Power, Separated Sense Pin		0.5~5.0		0.044			Yes			VDFx5%				
XC6134	Ta=-40~125℃, Hys Adj, Adj Release/Detect Delay Separate Sense pin	1.6~6.0	0.8~5.0	1.2%	1.32	CMOS Nch	Detect "H" Detect "L"	Yes	Adj	Adj	Adj	Yes	-	125℃	☑SOT-26 (2.9x2.8xh1.3mm) ☑USP-6C (1.8x2.0xh0.6mm)
XC6133			1.0~5.0								VDFx5%				
XC6132			0.8~2.0								Adj				
XC6127	Built in Release Delay, Manual Reset	0.7~6.0	1.5~5.5	0.8%	0.7	CMOS Nch	Detect "H" Detect "L"	-	-	50ms ~800ms	VDFx5%	Yes	-	85℃	☑SOT-25 ☑SSOT-24 USPN-4 (0.90x1.2xh0.4mm)
XC6126	High Accuracy	0.7~6.0	1.5~5.5	0.8%	0.7	CMOS Nch	Detect "L"	-	-	-	VDFx5%	-	-	85℃	☑SSOT-24 (2.0x2.1xh1.1mm) USPN-4B02(0.75x0.95xh0.4mm)
XC6119	Adj Release Delay	0.7~6.0	0.8~5.0	2.0%	0.9	CMOS Nch	Detect "L"	-	-	Adj	VDFx5%	-	CMOS Only	85℃	☑SSOT-24 (2.0x2.1xh1.1mm) ☑USPN-4 (0.90x1.2xh0.4mm)
XC6118	Separate Sense pin, Adj Release Delay	1.0~6.0			0.8			Yes			VDFx1% VDFx5%				☑SOT-25 (2.9x2.8xh1.3mm) ☑USP-4 (1.2x1.6xh0.6mm)

▷Middle Voltage Voltage Detectors : Input Voltage/Sense pin Voltage 10V or less

Product	Feature	V_{IN} [V]	V_{DF} [V]	Accuracy	Iq [μA]	Output		Voltage Detect						Topr max.	Package ☑ : Torex Longevity Program(TLP)
						Config.	Logic	Separate Sense Pin	Detect Delay time	Release Delay time	Hys	Manual Reset	Unstable operation prevention		
XC61C/XC61G	10V	0.7~10.0	0.8~6.0	2.0%	0.7	CMOS Nch	Detect "L"	-	-	-	VDFx5%	-	-	85℃	SOT-23, SSOT-24 SOT-89, USP-3 (1.2x1.2xh0.6mm)
XC61F/XC61H	10V, Built-in Release Delay	0.7~10.0	1.6~6.0	2.0%	1	CMOS Nch	Detect "L"	-	-	1ms ~400ms	VDFx5%	-	-	80℃	SOT-23 (2.9x2.8xh1.3mm) SOT-89 (4.5x4.0xh1.6mm)

▷High Voltage Voltage Detectors

Product	Feature	V_{IN} [V]	V_{DF} [V]	Accuracy	Iq [μA]	Output		Voltage Detect						Topr max.	Package ☑ : Torex Longevity Program(TLP)
						Config.	Logic	Separate Sense Pin	Detect Delay time	Release Delay time	Hys	Manual Reset	Unstable operation prevention		
FEATURED XC6138	VSEN pin 76V operation Hysterisis 5~50%, Adj Delay time	2.2~6.0	2.3~20.0	1.5%	0.5	CMOS Nch	Detect "H" Detect "L"	Yes	Adj	Adj	5~50%	Yes	-	125℃	☑SOT-25 (2.8x2.9xh1.3mm) ☑DFN1515-6A (1.5x1.5xh0.38mm)

▷Low Voltage Voltage Detectors with Watchdog function

Product	Feature	V_{IN} [V]	V_{DF} [V]	Accuracy	Iq [μA]	Output		Watchdog			Voltage Detect			Topr max.	Package ☑ : Torex Longevity Program(TLP)
						Config.	Logic	Timeout Period	Type	EN/ENB	Release Delay time	Hys	Manual Reset		
UNDER DEVELOPMENT XC6185-XC6188	RESET with Watchdog, EN Window WDT(XC6185-XC6188)	1.5 ~ 6.0	1.6 ~ 5.0	1.5%	3.5	Nch	Detect "L"	3.13ms ~1600ms	Yes	Yes	3.13ms ~1600ms	VDFx5%	-	125℃	☑SOT-25 (2.9x2.8xh1.3mm) ☑DFN1515-6A (1.5x1.5xh0.38mm)
XC6181-XC6184									-						
XC6131	Ta=-40~125℃, RESET with Watchdog, Adj Delay time	1.5~6.0	1.6~6.0	1.0%	2.5@EN=L 9.8@EN=H	Nch	Detect "L"	Adj	-	Yes	Adj	VDFx5%	-	125℃	☑SOT-26 (2.9x2.8xh1.3mm) ☑DFN1515-6A (1.5x1.5xh0.38mm)
XC6130					9.8					-			Yes		
XC6121-XC6124	RESET with Watchdog, EN Built-in Delay time	1.0~6.0	1.6~5.0	2.0%	10	Nch	Detect "L"	50ms ~1600ms	-	Yes	3.13ms ~400ms	VDFx5%	-	85℃	SOT-25 (2.9x2.8xh1.3mm) USP-6C (1.8x2.0xh0.6mm)